A Two-Stage 110VAC-to-1VDC Power Delivery Architecture Using Hybrid Converters for Data Centers and Telecommunication Systems

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Abstract—This paper presents a new power delivery architecture to bridge AC distribution voltages to core levels for computing loads using only 2 conversion stages with new converter topologies to potentially replace the traditional 4 stage structure in the development of new data centers. This paper also includes new converters as the solutions to the proposed two stages. A new switched-capacitor(SC) based AC-DC converter has been proposed for the first stage and demonstrated for 90V-110VAC to a 48-60VDC intermediate bus with power factor correction. The second stage is also an SC-based hybrid converter with multi-phase operation suitable for power delivery to the core voltages of ~1V with high current density. This work also reports a new phase sequence for the second stage for extended output voltage range. Individually, the first stage was measured at 96.1% peak efficiency for output currents ranging from 0-4.5A, while the second stage achieved 90.7% peak efficiency with a load range of 0-220A at 1V. Measured peak power densities are 73W/in^3 for the first stage and 2020W/in^3 for the second stage. In combination, the direct conversion from ~110 VAC to 1VDC achieves a peak efficiency of 84.1% while providing output currents up to 160A.

I. INTRODUCTION

Many industrial and household devices today receive power from AC power distribution lines, while many of them are actually DC loads by nature. These DC loads have been increasing fast and their power requirements have become ever more stringent in recent years. Particularly, modern data centers and telecommunications systems also fall into this category where the final loads are high-performance processors that need a group of power converters to interface with AC distribution lines [1]. With the demand for modern data processing power, computation, and storage requirements, these

processors have become excessively power-hungry which has ultimately translated into extremely high loading current at low supply voltages of ~1 V.

Conventionally, high-performance computing rack servers in data centers are powered from an AC grid through an isolation transformer, followed by an online Uninterruptible Power Supply(UPS), and typically four stages [1], [2] : 1) A power factor correction (PFC) rectifier from the AC line voltage to high-voltage DC link bus, 2) the second stage converts the DC link to intermediate DC bus at 48 V nominally, 3) a 48V-to-12V high-efficiency DC-DC conversion, and 4) the last stage converts 12 V to core voltages of 0.8 V to 3.3 V. This architecture is shown in Fig. 1a. Generally, isolation is required in only one stage from the grid to the core levels and a high power isolation transformer is used either before or after the UPS. As voltage conversion techniques in AC-DC and DC-DC applications are many times dependent on the transformers, transformers are also used in the last four stages, but they do not provide the safety-rated isolation required. The series connection of multiple stages also results in overall low power efficiency and density, leading to excessive heat which requires bulky and expensive cooling systems. As we are experiencing fast growth in data management and processing in recent days [3], [4], coupled with the introduction of 5G communications, artificial intelligence, crypto-currency, and cloud-dependent data processing and computations, this trend of power demand is only going to get more challenging. As a result, the traditional multiple power delivery architecture becomes a critical bottleneck of the system performance and cost and thus, should be replaced with more advanced, optimized, and efficient ones.

Improving power delivery and management plays a key role in minimizing the cost of building and operating future
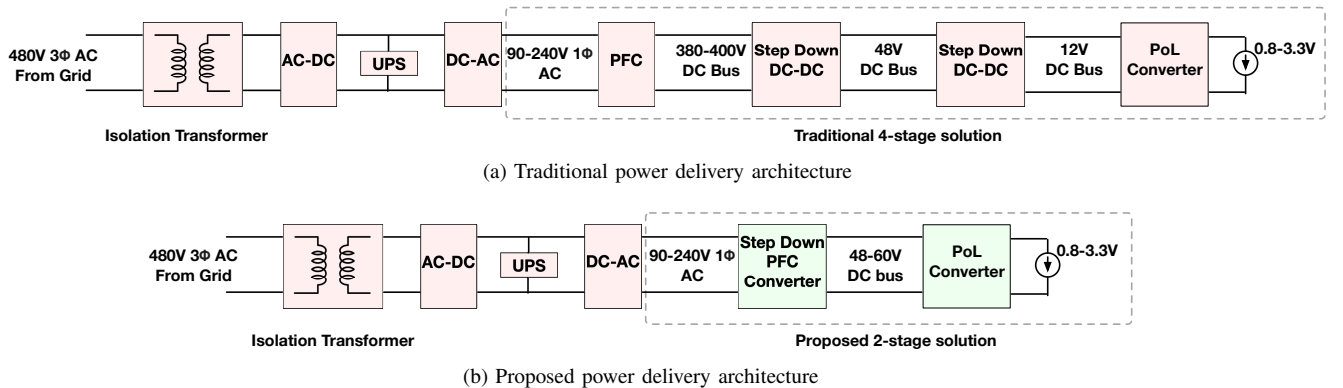

(a) Traditional power delivery architecture

(b) Proposed power delivery architecture

Fig. 1: Traditional and proposed Power Delivery Architecture

Step Down PFC Converter   **Multi-Phase Multi-Inductor Converter**
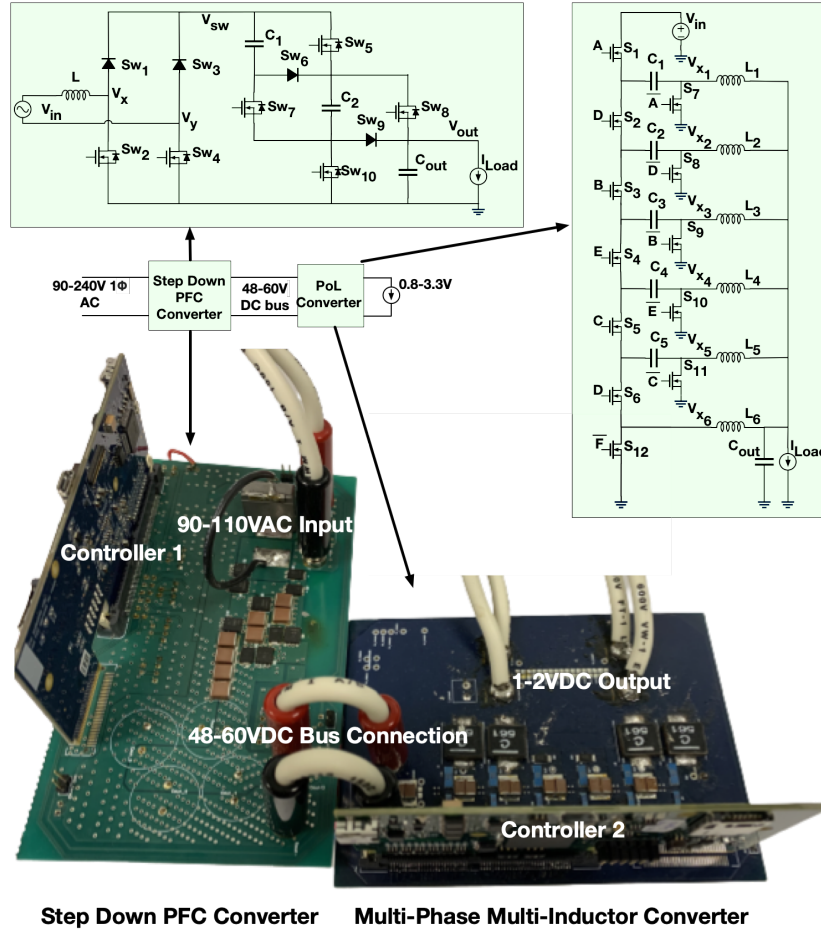
Fig. 2: New Power delivery architecture with stages implemented using new SC-based hybrid converters

green data centers to meet the fast growth of high-performance computing. Toward this important goal, a reduced number of conversion stages with large conversion ratio converters can be one of the most viable approaches to adopt simplifying the power delivery rack and improving efficiency. With this motivation, in this work we demonstrate an efficient distribution AC-to-core power delivery architecture for data centers and telecommunication systems comprised of only two direct conversion stages: 1) AC to 48-60V step-down PFC rectifier and 2) 48-60V to 0.8V-3.3V DC-DC converter stages. The proposed power delivery architecture is shown in Fig. 1b.

The two converter stages have been designed by employing hybrid converters that take advantage of both switched capacitor and inductor operations for better efficiency and power density. Full structure with device-level details are shown in Fig. 2. The PFC rectifier stage in this work utilizes a new multi-level hybrid converter based on partial series-parallel switched-capacitor operations to reduce inductor value and total harmonic distortion. It also steps down and moves the DC link to a lower voltage level, at 48-V nominal, where high-density capacitors can be utilized for energy buffer. Employing fast input current and slower output voltage control loops, this converter can simultaneously regulate the output voltage and input current to maintain good power factors and efficiency. The last-centimeter point of load (PoL) converter in this demonstration is a GaN-based multi-phase multi-inductor hybrid (MP-MIH) converter that was designed to provide very

high output currents at low voltages with very high current density. This paper is organized as follows. Section II and III discuss the PFC step down and the MPMIH converter in detail with operations and design considerations respectively. Section IV presents the experimental results. We will summarize and conclude the paper in Section V.

II. STEP DOWN PFC CONVERTER

Traditional AC-DC conversion with moderate to high power generally uses a bridge-less PFC converter [5], [6]. There are different control schemes adopted to regulate input current and output voltage to support the basic operation of this converter [7]. While this converter can achieve a very good displacement power factor or near zero phase lag between the input voltage and current, the distortion power factor can still deteriorate because of switching current ripple at high input voltages. Switching current ripple magnitude can be made smaller with larger input inductance, higher switching frequency, and/or lower voltage stress. While increasing the inductance requires a larger-sized inductor that leads to lower power density, increasing switching frequency may not be desirable because an optimal value is highly dependent on particular semiconductor devices and core materials of the inductor. From this consideration, topological modifications that allow smaller voltage stress on the input inductor and active devices can be a better solution to achieve the design goal.
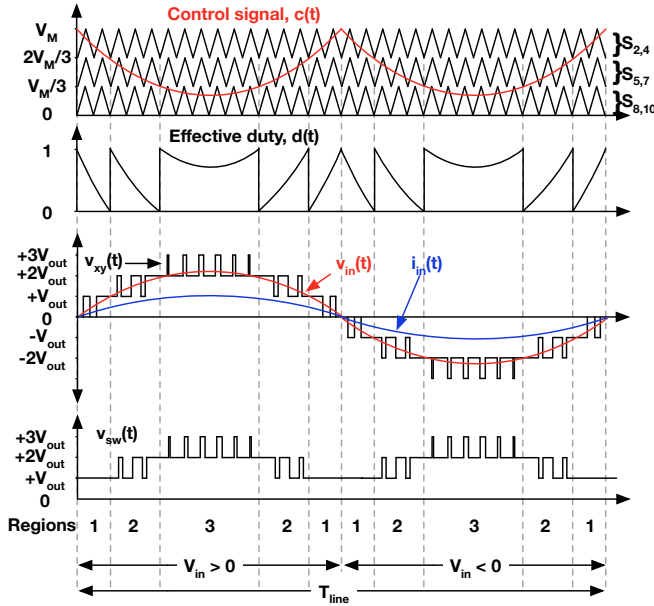
Fig. 3: Ideal operational waveforms

The modular multilevel converter has been popular for its topological advantages and is widely used in DC-AC applications. There are also reports on switched-capacitor architectures for conversion from a single DC voltage to a high voltage AC output [8]–[10]. However, the converter type is found much less explored in AC-DC conversion applications. In this work, the architecture of an S-hybrid converter [11] has been modified and merged with a bridge-less or totem pole PFC converter for AC-DC applications. The following section describes the topology and operation of the converter.

A. Topology and Operation

As shown in Fig. 2, the presented PFC step-down hybrid converter has one current shaping inductor, L, and four switches, Sw_{1-4} in the main rectifier. These switches operate at high frequency during the fraction of the line cycle at low voltage, while staying idle, on or off, for the remaining time. A switched-capacitor (SC) circuit follows the rectifier to provide the stepped-down output as well as multilevel switching voltages for the inductor. In this demonstration, the SC circuit has two flying capacitors C_{1-2} and six switches Sw_{5-10}. These switches also operate at the converter's operating frequency during designated periods of the line cycle.

Figure 3 depicts the simplified ideal operational waveforms of the full converter during a full line cycle. All capacitors are expected to have negligible voltage ripples and equal voltages. Assume an input voltage with a peak value of V_m

such that $2V_{out} \leq V_m < 3V_{out}$, the full line-cycle can be divided into three time regions: 1) region 1: $0 \leq |V_{in}| < V_{out}$ 2)region 2: $V_{out} \leq |V_{in}| < 2V_{out}$, and 3) region 3 : $2V_{out} \leq |V_{in}| < 3V_{out}$. For any of these regions, the converter switches are operated in such a way that, V_{xy} switches in a pulse-width-modulated (PWM) control manner between the upper and lower limit of the region to generate an average voltage equal to V_{in}. The rectifier switches, Sw_{1-4}, take care of selecting the right polarity of V_{xy} in accordance with the input voltage being positive or negative. As a result, V_{xy} switches among 7 levels (0, $\pm V_{out}$, $\pm 2V_{out}$ and $\pm 3V_{out}$).

The SC configurations to generate different switching node V_{sw} voltages suitable for different input voltage levels are shown in Figure 4. In operation, $Sw_{5,7}$ turn ON and OFF together while Sw_6 is their complementary switch. In a similar way, Sw_9 is the complimentary of $Sw_{8,10}$. The rectifier switches, Sw_{1-4} bridges the SC configurations with the input inductor and the source. In this proof of concept demonstration, $Sw_{1,3,6,9}$ are implemented with diodes for simplicity while $Sw_{1,2,5,7,8,10}$ are implemented with MOSFETs to control the operation of the converter. The switch selection for the main rectifier has been done following a standard bridge-less PFC converter design [5].

In order to control the switches, PWM control signals can be acquired by comparing a control signal c(t) with 3 separate carrier signals at 3 different voltage domains, as shown in Fig. 3. The control signal can be generated by weighing the regulation information of output voltage and input current in accordance with required output power and the input voltage. Particularly, when c(t) is in the first region, Sw_2 is switched at the carrier frequency when $V_{in}>0$, while switching of Sw_4 is activated when $V_{in}<0$. $Sw_{5,7}$ and $Sw_{8,10}$ are activated with c(t) in the second and third regions, respectively. In a practical implementation with digital PWM modules in a micro-controller, the effective duty cycle, d(t), can be calculated digitally based on similar information and used to generate the PWM signals. Following [11], d(t) can be calculated as:

$$d(t) = \begin{cases} 1 - \frac{|V_{in}|}{V_{out}} & \text{when, } 0 \leq |V_{in}| < V_{out} \\ 2 - \frac{|V_{in}|}{V_{out}} & \text{when, } V_{out} \leq |V_{in}| < 2V_{out} \\ 3 - \frac{|V_{in}|}{V_{out}} & \text{when, } 2V_{out} \leq |V_{in}| < 3V_{out} \end{cases} \quad (1)$$

Utilizing Eqn. 1 and assuming $V_M = 1$, a separate set of expressions for d(t) can be derived in terms of c(t) which is useful to directly generate the PWM signals for the switches using different PWM modules in the micro-controller:

$$d(t) = \begin{cases} 3c(t) - 2 & \text{when, } \frac{2}{3} \leq c(t) \\ 3c(t) - 1 & \text{when, } \frac{1}{3} \leq c(t) < \frac{2}{3} \\ 3c(t) & \text{when, } 0 \leq c(t) < \frac{1}{3} \end{cases} \quad (2)$$
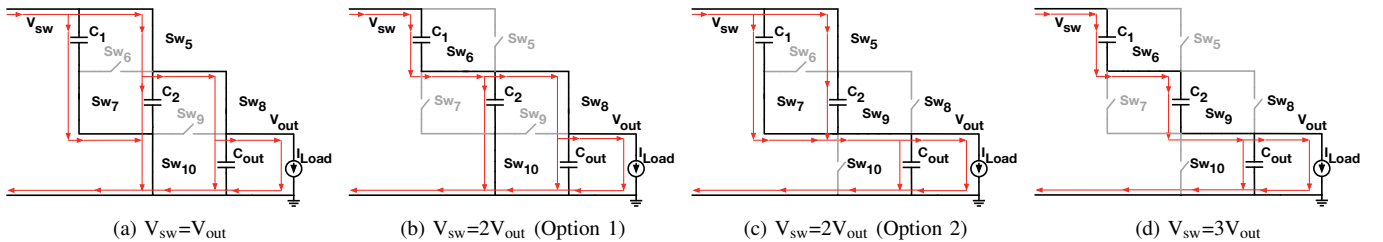

(a) $V_{sw}=V_{out}$ (b) $V_{sw}=2V_{out}$ (Option 1)   (c) $V_{sw}=2V_{out}$ (Option 2)   (d) $V_{sw}=3V_{out}$

Fig. 4: SC configurations to generate different switching node voltages

(a) Logical flow of the modified operation   (b) Practical implementation of the modified operation
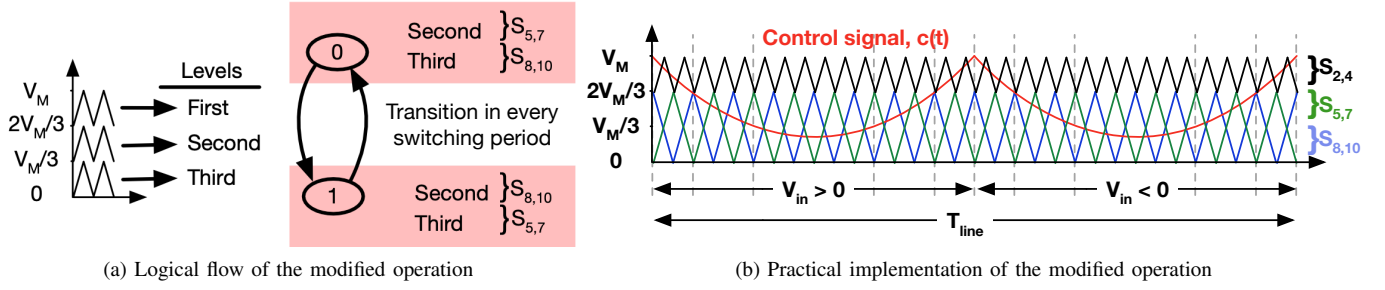
Fig. 5: Modified operation

Note that, the switches in the SC circuit block 3x times smaller voltages compared to the switches in the main rectifier. Therefore, these switches can be selected with a smaller voltage rating, lower $R_{DS,on}$, and lower parasitic capacitance to improve overall performance with reduced conduction and switching losses.

B. Modified Operation for Capacitor Balancing

In the operation described with Fig. 4, flying capacitors C_{1-2} and output capacitor C_{out} are placed either parallel or stacked in series to generated V_{out}, $2V_{out}$ and $3V_{out}$ levels at the switching node, V_{sw}. To generate $2V_{out}$, C_1 can be stacked on top of C_2 and C_{out} (configuration option 1) in Fig. 4b, or a parallel combination of C_1 and C_2 is placed on top of C_{out} in Fig. 4c (configuration option 2). Although theoretically capable of supporting the $2V_{out}$ needed for operation, using only one of these configurations causes high capacitor voltage ripple problem for capacitor C_1 and C_2 in region 3, where, V_{sw} is switched between $2V_{out}$ and $3V_{out}$. Particularly, if only configuration option 1 is used, C_1 keeps receiving charges without redistribution to lower capacitors as the converter stays in region 3. On the other hand, if only configuration option 2 is used, both C_1 and C_2 keep receiving charge without redistribution to C_{out} and the load. The excessive charge for the flying capacitor(s) in region 3 where the input current is at its peak will cause a high voltage ripple, significant hard-charging loss, and risks of over-voltage damages for both capacitors and active switches. In addition, the over-charged voltage in the flying capacitors also causes unwanted variations in the average voltage of V_{xy} which in turn distorts the current waveform, increasing current harmonics, and reducing the power factor.

The overcharging problem in flying capacitors was identified in [8] for a demonstration of an inverter with a slightly different topology and operation. It was also suggested to size the flying capacitor large enough to keep the over-voltage within a certain range. However, this method becomes less effective in high power applications where the input charging current is large, or very large capacitors are required. To avoid spending excessive area for more capacitance, in this work we introduce a relatively simple operational solution to solve this problem.

Recognizing that the key to the solution is charge redistribution among the flying capacitors and to the output capacitor, we combine and alternate both configurations, option 2 (Fig.
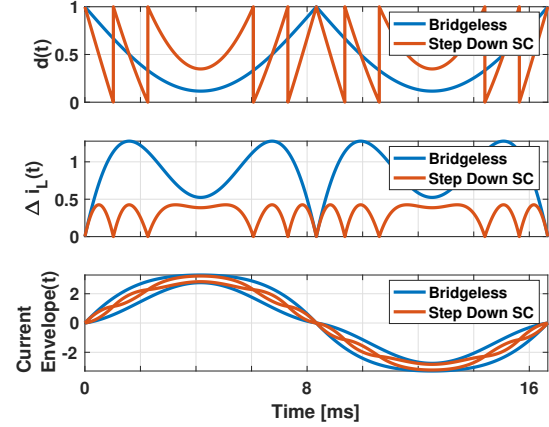

Fig. 6: Comparison of current ripples of the step-down PFC converter (90Vrms-to-48V/4A) and bridge-less PFC converter (90Vrms-to-3×48V/4/3A) for same output power operation with $47\,\mu$H inductor and $600\,$kHz switching frequency

4c) and option 1 (Fig. 4b), in each switching cycle to generate $V_{sw}=2V_{out}$. In this way, the input charge is redistributed to the load every two switching cycles.

To implement this modified control, simple logic conditions can be added to generate alternative PWM signals from the second and third levels of multilevel carrier signals in Fig. 3 for $Sw_{5,7}$ and $Sw_{8,10}$. These conditions can be active for the full line cycle without changing the basic operation of the converter. Fig. 5a depicts the simplified logical diagram for the modified operation.

To generate these control signals with a smooth transition between different regions in a more practical implementation in a micro-controller, carrier signals can be modified as in Fig. 5b, where the second and third carrier signal levels are implemented with two 180°phase-shifted PWM signals with magnitudes from 0 to $2V_M/3$. In this way, at least once in every two switching periods, C_1 is placed in parallel to C_2 and C_2 is placed in parallel to C_{out}, which is tightly regulated. This operation makes sure the flying capacitors closely track the regulated output voltage V_{out} as frequently as every other switching cycle.

It is worth noting that, this over-voltage problem does not come into the scene during regions 1 and 2 as charge redistribution to C_{out} and V_{out} happens once in every switching period, keeping an equal voltage for all the capacitors, $V_{C_1} = V_{C_2} = V_{C_{out}} = V_{out}$. Also, the increased voltage for C_1 in this converter is different than the imbalance problem
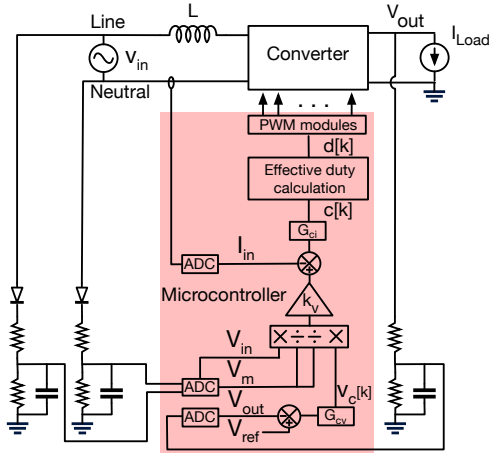
Fig. 7: Controller with sensing circuits

in FCML converters. The resultant voltage variation in this converter is at line frequency, does not depend on small timing mismatches [12], and can be calculated quite precisely with existing models.

C. Advantage of the Proposed Converter: Reduced Inductor Current Ripple

With two flying capacitors and an output capacitor, this converter can generate seven levels for V_{xy} node voltage. As a result, in a major portion of the line cycle, the inductor is charged and discharged by a smaller amount of voltage compared to a bridge-less or totem pole PFC converter. Particularly, in region 1, the inductor is switched to either input voltage or V_{out} which is smaller than V_m. In region 2, the inductor voltages are $|V_{in}|$-V_{out} and $2V_{out}$-$|V_{in}|$, while in region 3, they are $|V_{in}|$-$2V_{out}$ and $3V_{out}$-$|V_{in}|$. Using the inductor voltage information, the current ripple of the step-down PFC converter is calculated and compared with a bridge-less/totem-pole PFC converter at the same power and operating point in Fig. 6. It can be observed that the new step-down PFC converter maintains smaller current ripples and thus, a narrower envelope of the inductor current throughout the operation. Hence, one can also predict a superior THD performance in the new converter compared with a bridge-less/totem-pole PFC converter at the same operating condition.

D. Advantage of the Proposed PFC Converter: DC-Link Filtering with Distributed Low-Voltage Capacitors

In any AC-DC or DC-AC application, the choice of total DC link capacitance depends on the line frequency, maximum power, and maximum allowed voltage ripple. The amount of capacitance is typically very large considering large output power and low line frequency. The presented step-down PFC converter also falls in this general category. However, different from conventional PFC converters, this converter carries out the DC-link filtering function at the low-output voltage levels. More importantly, the switched-capacitor operation with efficient charge redistribution, described in subsection II-B, allows all flying capacitors and output capacitor to participate as DC-Link capacitors. A key benefit here is that this allows the large DC-Link capacitance to be distributed among the flying

capacitors with no difference in energy buffering performance. As an additional benefit, large values of flying capacitors minimize their switching-frequency ripple and hard-charging loss to improve overall efficiency. The low output voltage rating requirement also enables the selection of higher-density capacitors to reduce overall implementation size and increase the system power density.

As a design aspect, one needs to select between electrolytic and ceramic capacitors for the converter. The design can be made electrolytic-free by using ceramic capacitors either with or without methods to enhance the energy buffering capability of the capacitors, for example, using a series stacked energy buffer [13] or stacked switched capacitor buffer [14]. While there are certain benefits in an electrolytic-free implementation, the main drawback associated with using only ceramic capacitors for both flying and output capacitors is that they are more expensive and have relatively lower energy density compared with electrolytic capacitors.

E. Control and Sensing Circuits

The traditional feed-forward average current mode control for the PFC boost converter has been employed to control this new converter [7]. Figure 7 illustrates the block diagram of the control procedure in a micro-controller. While the controller ground has been chosen as the negative terminal of the converter's output, it simplifies the sensing of the output voltage. For input voltage sensing a simple rectifier followed by a resistive divider has been chosen to provide the magnitudes of the input voltage to the controller through an analog to digital conversion. A Hall-effect sensor has been used for current sensing purposes.

Small-signal model analysis of the converter's input current response and output voltage indicates the converter behaves the same way as multi-level converters and standard PFC boost converters [15]. Thus, the long-existing and well-adopted knowledge for the control of a PFC boost converter can readily be used to design the voltage compensator, G_{cv} and current compensator, G_{ci}. Detailed steps for this design can also be found in [7] and thus have not been included here. Delay-associated poles from the micro-controller have also been considered to properly design the compensators [16].

III. Multi-phase Multi-Inductor Hybrid Converter

Recently, the last stage converter for 48V-to-1V conversion has received a lot of interest in industry and academic research with remarkable implementations using both isolated [17], [18] and non-isolated architectures [19]. In this work, we utilize a member of the multi-inductor hybrid (MIH) converter family [20]–[24], a 6-level converter extension of the previously demonstrated DP-MIH converter reported in [24]. The additional inductors and interleaved phases are extended to support larger output currents compared with prior works.

A. Multi Inductor Converter with Multi-Phase Operation

The 6-level MP-MIH converter is depicted in Fig. 2. It has twelve switches S_{1-12}, five flying capacitors C_{1-5} and six
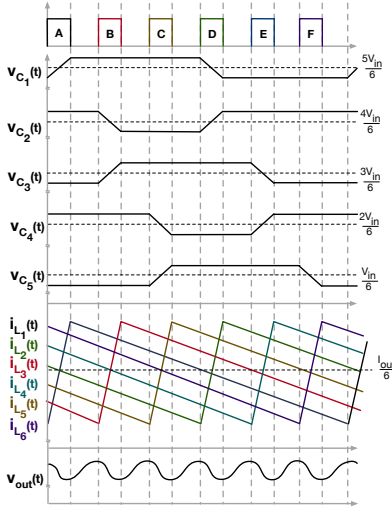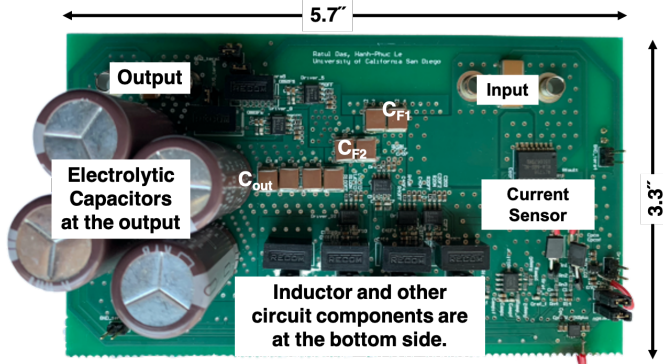
Fig. 8: 6-level multi-phase multi-inductor (MP-MIH) hybrid converter and its operation with AD-BE-CF phase sequence
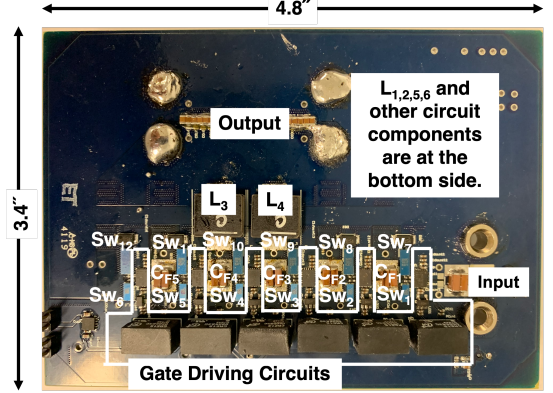
TABLE I: Components used in PFC step down converter

Components	Part Number
$Sw_{1,3}$	SBR10U200P5DICT-ND
$Sw_{2,4}$	BSC500N20NS3GATMA1CT-ND
$Sw_{5,7,8,10}$	BSC123N08NS3GATMA1
$Sw_{6,9}$	SBRT20M80SP5-13
$C_{1,2}$	8xC5750X7S2A156M250KB
C_{out}	8xC5750X7S2A156M250KB+ 4xEKYB101ELL102MM40S
L	IHLP6767GZER470M11
Gate driver	UCC5350MCDR
Current Sensor	ACS716KLATR-6BB-NL-T

TABLE II: Components used in MPMIH converter

Components	Part Number
Sw_{1-6}	2xEPC2015c
Sw_{7-12}	2xEPC2023
C_{1-5}	4xCGA8M3X7S2A335M200KB
L_{1-6}	XAL1030-561ME
Gate Driver	LMG1210

(a) Step-down PFC multi-level AC-DC converter

(b) 6-level MP-MIH DC-DC Converter using GaN FETs

Fig. 9: Two converter prototypes of the 110VAC-to-1VDC power delivery architecture

inductors L_{1-6}. The input switched-capacitor (SC) network divides the input voltages by 6 times to feed into the Buck-like output filter inductors that, in turn, synchronously soft-charge and soft-discharge the flying capacitors. The high-side six switches S_{1-6} are controlled by six multi-phase pulse width modulated (PWM) signals, A-F with duty cycle, D, while the ground-connected freewheeling switches S_{7-12} are controlled by six complementary signals, $\overline{A}$-$\overline{F}$, respectively. Accordingly, the output voltage and flying capacitor C_i voltages can be represented by $V_{out} = \frac{DV_{in}}{6}$ and $V_{C_i} = \frac{6-i}{6}V_{in}$ where $i = 1-5$. The key constraint in the converter operation is that no two consecutive signals controlling two consecutive high-side switches in S_{1-6} can overlap. Following this constraint, the converter can support an operation of two to six interleaving phases with the six inductors of the six-level converter. While a maximum number of phases yields advantages in output voltage ripple and transient response as well as switching loss reduction, it also limits the maximum duty cycle and thus maximum output voltage. For example, six phases are non-overlapped and evenly distributed with $60°$ phase shift and A-F are arranged for the switches Sw_{1-6} sequentially, each of the phases A-E has a maximum duty cycle of $1/6$, limiting the maximum output voltage to $V_{in}/36$. However, it is also possible

to arrange the phases in a different, non-sequential method to allow a larger maximum duty cycle while still satisfying the requirement of no overlap in consecutive phases. Figure 8 depicts an example operation where steady-state operation of the MP-MIH converter using this strategy. The six non-overlapped phases, in the order of A to F, are limited to $3/6$, $2/6$, $2/6$, $3/6$, $3/6$, and $3/6$ respectively. This arrangement allows a maximum output voltage $V_{in}/18$ while still obtaining the benefits of a 6-phase interleaving operation with equal duty cycles. When a maximum output voltage is prioritized, the converter operation can be changed to 2-phase interleaving to reach an output voltage of $V_{in}/12$.

IV. EXPERIMENTAL RESULTS

The two-stage 110VAC-to-1VDC power delivery architecture has been implemented using two converter prototypes, shown in Fig. 9a and 9b. Key components for the converters are listed in Table I and II. These converters have been tested separately and in combination to demonstrate the full structure.

A. Step-down PFC Converter

Figure 10 shows the key waveforms of the converter at 90VAC to 48V/4A operation. It can be seen that the input
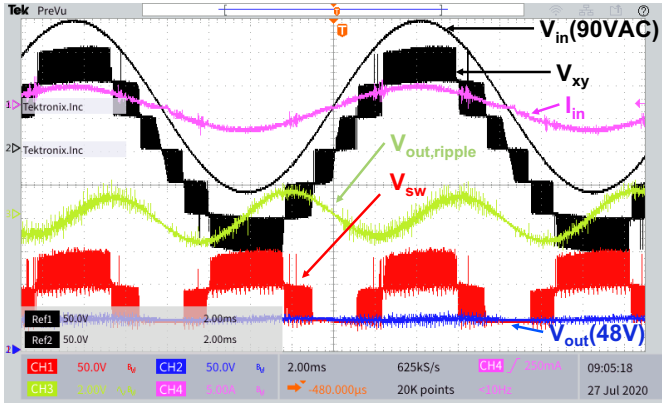
Fig. 10: Steady state waveforms at 90Vrms to 48V/4A operation of the step down PFC converter

Fig. 11: Experimental waveforms of I_{L1}, I_{L_2} and V_{C1} in MPMIH converter [at 48V to 2V/40A conversion at 300kHz with AD-BE-CF phase sequence]

current follows the input voltage, verifying the key PFC operation. The performance of the converter is shown in Fig. 13 in terms of efficiency and power factor. The converter maintains higher than 96% efficiency for a wide range of operations and more than 95% for almost all operating points. As shown in Fig. 13b, the converter achieve a power factor of 0.98 at 2.6 A effective input current. The power factor goes down at lower input current, i.e. lower output power, because of noise and harmonics caused by multi-level switching operations that couple to and reduce the accuracy of the current sensor and the current regulation loop. The power density of this converter at the full power is 73W/in^3, including all the components including output electrolytic capacitors.

B. MP-MIH Converter

Figure 11 and 12 shows the key waveforms of the MPMIH converter in a 48V to 2V/40A operation example. Using a phase sequence selection presented in Fig. 8, the converter's output current was a 6-phase interleaved combination of inductor currents. The standalone performance of this converter is presented in Fig. 14. At 48V-to-1V operation this converter achieved a peak efficiency of 90.75% at 40A load current, whereas, 92.31% efficiency was achieved for a 48V-to-1.8V conversion and at 50A output current. The converter was tested to a maximum load current of 220 A at 1V and 240 A at 1.2-1.8V. Considering the components in the power flow path, this converter achieved current density of 1.03 kA/in^3 for 1V and 1.123 kA/in^3 for other output voltages which translates into 1.03 kW/in^3 and 2.02 kW/in^3 peak power densities for 1V and 1.8V output voltages, respectively. Similar experiments have also been carried out for 54V input voltage. At 54V input voltage, this converter achieved peak efficiency of 90.6% and 92% for 1V and 1.8V output voltage, respectively.

C. Full System Verification

The MP-MIH converter was connected to the step-down PFC converter's output to complete the full power delivery system that bridges an AC distribution voltage to core DC voltages. Figure 15 shows the operations of the full system in line and load transients. The waveforms of input inductor
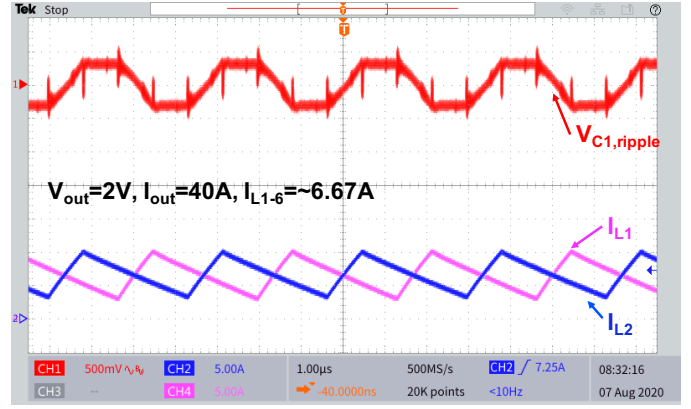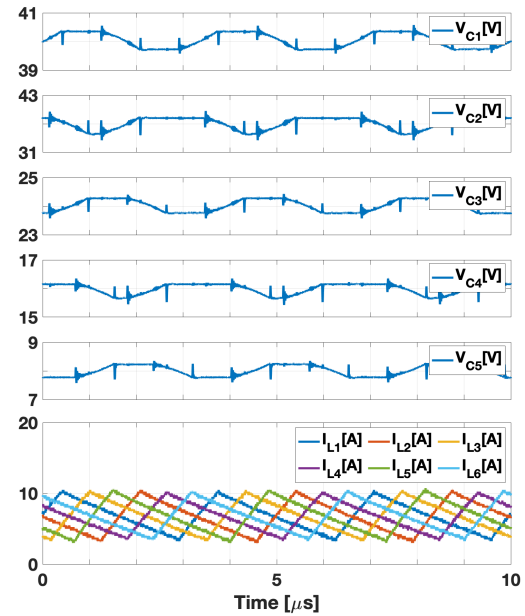

Fig. 12: Measured capacitor and inductor waveforms of the MP-MIH converter prototype for 48V to 2V/40A operation

current (I_{in}), output current ($\frac{I_{out}}{4}$), switching voltage (V_{sw}), and output voltage (V_{out}), illustrate stable operations and regulations of the converter and output voltage when the converter is exposed to a 40 Vrms line voltage step (Fig. 15a) and a 50A load step ((Fig. 15b). The first-stage step-down PFC hybrid converter can provide a fast response toward big line transients thanks to the flying capacitors capable of changing multiple levels, while remaining variations at the output of the first stage are managed by the second stage regulation. The seamless duty cycle control from the second stage also takes care of the high load current transient at the final output. The overall efficiency of the system is shown in Fig. 16. For 110VAC-to-1VDC operation, the overall efficiency peak is 84.1%. The peak output current when testing the full system is limited to 160A because of a non-fundamental limit in the design of the first-stage AC-DC converter which has an output current under 4.5A.

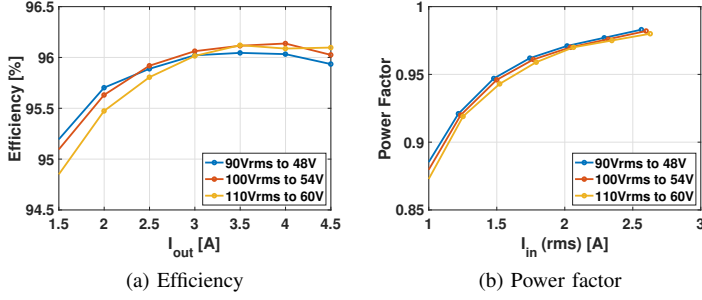For comparison, a conventional power delivery architecture

(a) Efficiency

(b) Power factor

Fig. 13: Performance of the step-down PFC Converter
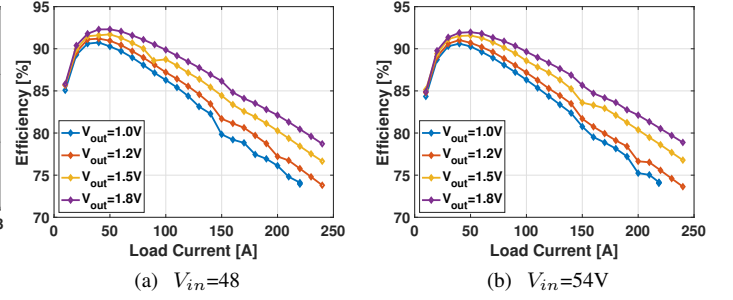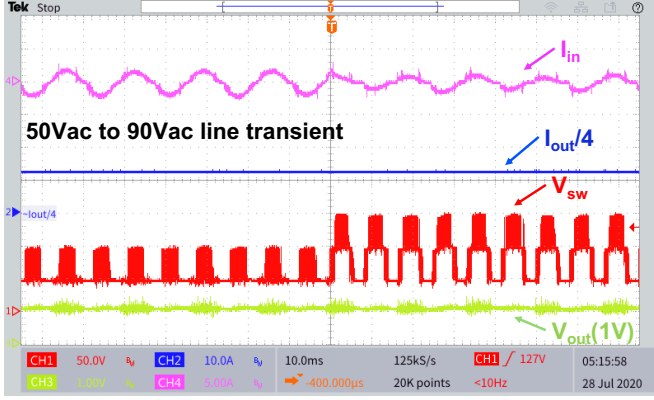

(a) V_{in}=48

(b) V_{in}=54V

Fig. 14: Efficiency of the MP-MIH converter

(a) Operation at 1V/50A for a 50Vrms to 90Vrms line transient

(b) Operation at 1V from 90Vrms input voltage for a 50A to 100A load transient

Fig. 15: Measured waveforms of the complete two-stage architecture for line and load transients
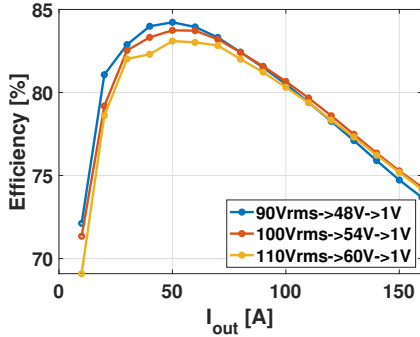

Fig. 16: Efficiency of the full AC Grid-to-Core voltages system

using 4 conversion stages for the same application would require all stages to individually achieve, on average, an efficiency of 95.8% to reach an equivalent performance of this proposed two-stage architecture. Considering the full conversion of from 110 VAC to 1 VDC, to the authors' best knowledge this has not been demonstrated.

V. CONCLUSION

In this work, we have successfully demonstrated the first two-stage architecture to directly convert AC distribution voltage to the core voltages that can be applied to power delivery in data centers and telecommunication systems. The demonstration includes a new switched-capacitor multi-level step-down PFC converter and a 6-level switched-capacitor-based multi-phase multi-inductor hybrid (MPMIH) converter. The

operation of the step-down PFC converter was discussed with control mechanisms for output voltage and input current regulations. A simple method of charge redistribution for flying capacitor voltage balancing at the carrier switching frequency was also provided. In designing the MP-MIH converter, a new phase sequence has been proposed and verified in experiments for larger output voltage and current ranges. The converter designs are verified separately and together in the complete two-stage AC grid-to-Core voltage system, demonstrating a bright promise for future applications to contribute to more green and energy-efficient data centers, telecommunication, and other IT systems.

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