Double Synchronous Unified Virtual Oscillator Control for Asymmetrical Fault Ride-Through in Grid-Forming Voltage Source Converters

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***Abstract*—A double synchronous unified virtual oscillator controller (dsUVOC) is proposed for grid-forming voltage source converters to achieve synchronization to the fundamental frequency positive- and negative-sequence components of unbalanced or distorted grids. The proposed controller leverages a positive- and a negative-sequence virtual oscillator, a double-sequence current reference generator, and a double-sequence vector limiter. Under fault conditions, the controller enables to clamp the converter output current below the maximum value limited by the converter hardware while retaining synchronization without a phase-locked-loop (PLL) regardless of the balanced or unbalanced nature of grid faults. Consequently, balanced and unbalanced fault ride-through can be achieved without the need for switching to a back-up controller. The paper presents the systematic development of the double-synchronous structure along with detail design and implementation guidelines. Validation of the proposed controller is provided through extensive control-hardware-in-the-loop (CHIL) experiments.**

***Index Terms*—Double synchronous unified virtual oscillator control (dsUVOC), asymmetric fault ride-through, unbalanced fault ride-through, positive and negative sequence synchronization, grid-forming converter, unified virtual oscillator control (uVOC)**

NOMENCLATURE

L_1, L_2, C_f	LCL filter components.
v_c	Converter switch-terminal output.
v_r	Controller output voltage.
i_1	Converter-side current.
i_2	Grid-side current.
v_{poc}	Converter terminal voltage.
Z_{g1}, Z_{g2}	Grid impedances.
Z_F	Fault impedances.
P_0	Real power set-point.
Q_0	Reactive power set-point.
V_0	Nominal voltage (L-N RMS) set-point.
ω_0	Nominal frequency set-point.
v	Oscillator output voltage.
i	Input current to oscillator.
η	Synchronization gain.
μ	Magnitude correction gain.
R_0	Active resistance.
i_0	Current reference.
$\underline{i}_0$	Saturated current reference.
N	Number of phases.
x_f	Fault flag.
x_r	Mode transition signal.
V_T	Under-voltage threshold.
I_m	Maximum current limit.
v_{TH}	Equivalent grid/network voltage.
Z_{TH}	Equivalent grid/network impedance.
ω	Equivalent oscillator frequency.
ω_g	Grid frequency.
δ	Power angle.
Z_v	Virtual impedance.

Boldface notation is used to indicate space vectors in stationary $\alpha\beta$ frame; complex vector and column vector notations such as $\mathbf{i} = i_\alpha + ji_\beta = [i_\alpha \ i_\beta]^T \leftrightarrow [i_a \ i_b \ i_c]^T$, are used interchangeably. Capital letters such as I are used for root-mean-square (RMS) values and $\hat{(.)}$ denotes the peak value such as $\hat{I}$; $\underline{(.)}$ denotes saturated/ limited value by the controller. Positive and negative sequence components of a variable/ quantity/ parameter are represented by the respective notations with $+$ and $-$ in the subscript. $\|(.)\|$ denotes the Euclidean norm such as $\|(\mathbf{i})\| = \sqrt{i_\alpha^2 + i_\beta^2}$.

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I. INTRODUCTION

Grid-forming (GFM) converters are believed to be the key enabling technology for high penetration of power electronics interfaced distributed generation into the power system [1], [2]. As opposed to the *current-source* nature of conventional grid-following (GFL) converters, GFM converters are programmed to emulate a *voltage behind reactance* response. Consequently, despite their superior grid-supporting features such as voltage and frequency regulation and inertial support, GFM converters are prone to transient over-current under fault conditions. Due to their current-source behavior, GFL converters provide excellent over-current limiting response, whereas without explicit fault management measures, GFM converters may experience excessive over-currents leading to hardware damage. Ride-through of symmetrical and asymmetrical faults remain one of the key challenges for GFM converters till date.

Early works on fault ride-through (FRT) by GFM converters rely on a separate set of back-up controller which employs phase-locked-loop (PLL) based vector current controllers; a controller switch is performed as soon as a fault is detected [3]–[5]. To eliminate such controller switch under fault conditions, another class of FRT strategies have been proposed for

GFM controllers consisting of cascaded voltage and current reference tracking loops beneath the real and reactive power control loops [6]. In this class of FRT controllers, explicit limits are imposed on the references to the inner current tracking loops to prevent excessive over-current under faults. However, this approach is prone to *integral windup* issues in the outer voltage and power control loops. In essence, under such scenarios the *power synchronization* action through transient transfer of active and reactive powers by the outer loops is cut-off due to windup and consequently synchronization is lost [7], [8]. A potential solution was presented in [8], where a proper coordination between the inner loops and the outer power control loops is used to prevent such windup phenomena. Another class of FRT controllers have also emerged which avoid such windup by means of dynamic virtual impedance [9], [10]. However, to fully utilize the converter's current capability the required virtual impedance is dependent on the variable grid condition during fault, such as the depth of voltage sag and/or phase jump and grid impedance. An explicit current limiter provides a more intuitive and easier implementation [8].

Virtual oscillator based controllers, such as virtual oscillator control (VOC) and dispatchable virtual oscillator (dVOC), are another class of emerging GFM controllers which are designed for almost global synchronization guarantee in arbitrary N-converter networks with zero inertia [11]–[14]. These nonlinear time-domain controllers provide substantially faster synchronization compared to synchronous machine emulation based methods such as droop control and virtual synchronous machine (VSM) [15]. A unified virtual oscillator controller (uVOC) was recently proposed which inherits the rigorous theoretical foundation and asymptotic synchronization guarantee of dVOC and provides enhanced ride-through capability under symmetrical grid faults [16], [17]. Unlike conventional droop based methods, uVOC uses explicit current references in the power-synchronization loop, which offers a unique advantage for limiting over-current; current-limiters can be embedded directly in the synchronizing controller. Consequently, symmetrical FRT is achieved without the need for controller switch and/or dynamic virtual impedance. Furthermore, uVOC exhibits a first-order power-angle response [17], [18], i.e., fault-recovery is not constrained by any critical clearing angle (CCA) which constrains second-order controllers such as droop control and VSM.

Although, majority of reported literature focus on symmetrical FRT, asymmetrical faults, such as single-line-to-ground (SLG) and double-line-to-ground (DLG) faults, are more frequent in real systems. Asymmetrical FRT strategies for GFL converters have been developed from the primary motivation of protecting the converter hardware from excessive current stress and/or power oscillation [19]–[21]. In most GFL applications, these asymmetrical FRT strategies rely on a decoupled double synchronous reference frame phase-locked-loop (DDSRF-PLL) for synchronization to the fundamental frequency positive- and negative-sequence components of the unbalanced grid; vector current controllers are used in both sequences to limit the converter output current. A number of current reference generation schemes have been reported for different control objectives such as balanced current injection and constant real power flow. Asymmetrical FRT in GFM applications can be achieved by switching to a DDSRF-PLL based vector current controller under fault. However, synchronization issues of PLLs, specifically under weak grids, have been well-documented in literature [16], [22]. A number of PLL-free asymmetrical FRT approaches have been reported. In [9], instead of synchronizing to the unbalanced grid, pre-fault values of the frequency and voltage magnitudes are used under faults. In [23], [24], two set of current controller are used beneath the power control loops to limit the positive- and negative-sequence currents. In [10], the outer power control loops synchronize to the positive-sequence voltage while an adaptive virtual impedance combined with inner voltage and current control loops are used to limit output current under asymmetrical faults. Another class of asymmetrical FRT controllers have been proposed for GFM converters, which employ *power-synchronization* in both positive and negative sequences [25]–[27]. These early attempts focus on protection of the converter hardware through balanced power control and/or active power oscillation. However, detail implementation guidelines and performance evaluation under realistic fault conditions have not been reported. Furthermore, no compatible asymmetrical FRT methods have been reported for oscillator based GFM controllers.

In this work, a double synchronous unified virtual oscillator controller (dsUVOC) is developed which employs two oscillators to achieve power synchronization to both positive- and negative-sequence fundamental frequency components of an unbalanced or distorted grid. Over-current limiting under fault conditions is achieved by integrating a double-sequence vector limiter on the sequence-current references used by the synchronizing oscillators. FRT under symmetrical or asymmetrical fault conditions with over-current limiting as well as voltage support and unbalance mitigation are achieved without the need for switching to a back-up controller or a PLL. The rest of the paper is organized as follows: first, the grid-tied VSC system of interest is presented. Second, the proposed dsUVOC structure is introduced. Third, the principle of operation through power synchronization in both sequences is explained. Fourth, control hardware-in-the-loop (CHIL) test results are presented to validate the proposed controller.

II. Asymmetrical FRT in Grid-Tied VSCs

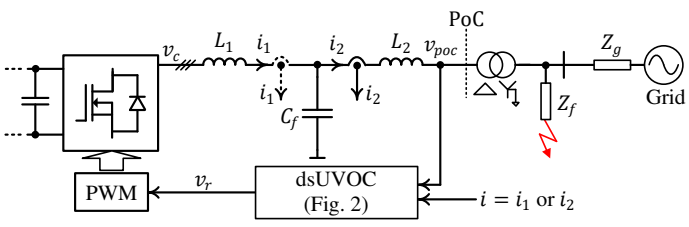

Figure 1. Grid-tied converter under study; red arrow denotes fault location at upstream of the Δ-Yg feeder transformer.

Fig. 1 shows a grid-tied VSC fed by a Δ-Yg transformer. The converter operation under upstream asymmetrical faults,

marked by the red arrow, is of interest. Such asymmetrical faults can be classified into two types - faults which result in only voltage sags at the point of coupling (PoC), such as single-line-to-ground (SLG) faults and faults leading to voltage sag accompanied by phase jump at the PoC, such as double-line-to-ground (DLG) faults. Note that the Δ feeder connection prevents zero-sequence currents at the PoC, and hence only positive- and negative-sequence fault currents are of interest. Effective FRT is motivated by an underlying converter-oriented or system-oriented objective, constrained by the hardware capability, and must be enabled by an appropriate controller.

Under fault conditions, the overall control objective may vary in different applications and is set by a higher-level coordinator. For instance, converter-oriented FRT objective may be tailored to reduce stress on the converter hardware by minimizing active power oscillation, i.e., constant active power injection, or to equalize loading of all three phases, i.e., balanced current injection. System-oriented FRT objectives may be set to provide terminal voltage support at the PoC and/or unbalance mitigation. Naturally, converter-oriented FRT objectives are favored by manufacturers, whereas system operators may mandate system-oriented FRT objectives. However, relevant standards for desired FRT response by GFM converters are still under development and the lack of clear guidelines have led to different ride-through strategies. Standardization of such FRT objectives/responses requires extensive system-level research and consensus among various stakeholders such as converter manufacturers and system operators. Optimization of FRT objectives, such as optimum real and reactive power references for converter vs. system oriented objectives, are kept out of scope in this work. Instead, we focus on the FRT controller to enable flexible control capability for various converter-level and system-level objectives while respecting the hardware constraints.

Irrespective of the underlying objective, the hardware current capability/constraint must be respected during the FRT operation. Overall, for effective FRT, the controller must have two key capabilities; first, synchronization to the positive- and negative-sequence components of the asymmetric grid. Synchronization to only the positive-sequence component may suffice for specific converter-oriented objectives such as balanced current injection; however, more demanding objectives such as constant active power injection and voltage unbalance mitigation at PoC require synchronization to both positive- and negative-sequence grid voltage components. Second, fast overcurrent limiting is essential, specially when fault occurs and is cleared. Finally, proper coordination between the controller elements responsible for synchronization and for saturating output current is essential to retain synchronism under current-limited operation. The following section describes the proposed dsUVOC structure followed by detailed explanations of how the various control capabilities are achieved.

III. Double Synchronous Unified Virtual Oscillator Control

The dsUVOC implementation in a grid-tied VSC is shown in Fig. 1 where either the converter-side i_1 or the grid-side current i_2 feedback can be used. No voltage or current reference tracking loops are used; the dsUVOC output is directly used by the pulse-width-modulator (PWM). The detail dsUVOC structure is shown in Fig. 2, which consists of a positive-sequence space vector oscillator (SVO), a negative-sequence SVO, a double sequence current reference generator, and a double sequence vector limiter. Furthermore, an active resistance R_0 and virtual impedance $Z_v(s)$ are used. Next, the different components of the controller are described in the following subsections.

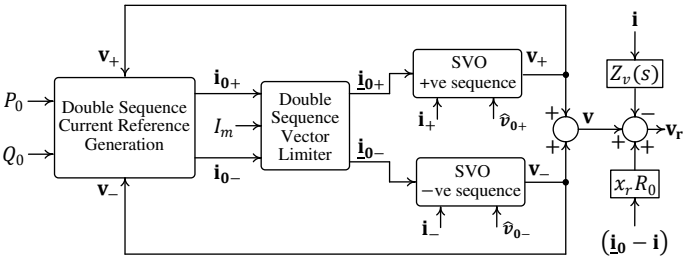

Figure 2. Proposed double synchronous unified virtual oscillator controller.

A. Positive- and Negative-Sequence Space Vector Oscillators

Historically, the bulk power system has relied on a very simple and natural synchronization process among large synchronous machines/generators. A traditional generator is designed to operate at the synchronous speed/frequency, such as 60Hz in the United States, when the nominal real power is drawn from its output terminals. While connected to an electrical grid, any increase (decrease) in a generator's operating speed with respect to the synchronous frequency of the grid leads to an increase (decrease) in its output power. An increase (decrease) in output power forces the generator to slow down (speed up). Thus, a generator achieves self-synchronization with the rest of the electrical grid through a transient exchange of power; this natural synchronization process through power-frequency drooping is termed as *Power Synchronization*. Power synchronization is leveraged as the fundamental synchronizing mechanism in synchronous machine emulation based GFM control approaches such as droop control, PSC, and VSM. In [16], uVOC was shown to exhibit instantaneous power vs. frequency droop response which demonstrated the power synchronization nature of uVOC. In this work, the proposed dsUVOC leverages power synchronization in both positive- and negative-sequences to achieve synchronization to the fundamental-frequency sequence components of an unbalanced/distorted grid. The positive- and negative-sequence SVOs serve as the synchronizing units and are implemented as

$$\dot{\mathbf{v}}_+ = j\omega_0 \mathbf{v}_+ + j\eta_+(\underline{\mathbf{i}}_{\mathbf{0}+} - \mathbf{i}_+) + \mu_+(\hat{V}_{0+}^2 - \|\mathbf{v}_+\|^2)\mathbf{v}_+, \tag{1}$$

$$\dot{\mathbf{v}}_- = -j\omega_0 \mathbf{v}_- - j\eta_-(\underline{\mathbf{i}}_{\mathbf{0}-} - \mathbf{i}_-) + \mu_-(\hat{V}_{0-}^2 - \|\mathbf{v}_-\|^2)\mathbf{v}_-. \tag{2}$$

The current references $\mathbf{i_{0+}}$ and $\mathbf{i_{0-}}$ are generated from the SVO outputs $\mathbf{v}_+$ and $\mathbf{v}_-$ following the guidelines presented in Section III-B. The sequence current components $\mathbf{i}_+ = i_{\alpha+} +$

$ji_{\beta+}$ and $\mathbf{i}_- = i_{\alpha-} + ji_{\beta-}$ of the converter output current $\mathbf{i} = i_\alpha + ji_\beta$ are extracted as

$$\begin{aligned} \mathbf{i}_{\alpha+} &= 0.5(i_\alpha - i_{\beta\perp}); \quad \mathbf{i}_{\beta+} = 0.5(i_\beta + i_{\alpha\perp}), \\ \mathbf{i}_{\alpha-} &= 0.5(i_\alpha + i_{\beta\perp}); \quad \mathbf{i}_{\beta-} = 0.5(i_\beta - i_{\alpha\perp}). \end{aligned} \tag{3}$$

Here, $(.)_\perp$ denotes the orthogonal version of the respective signal obtained by delaying the original signal by $T_0/4$, where T_0 is the fundamental period. The synchronization and magnitude correction gains are set as

$$\eta_+ = \eta_- = (1 + x_r/\tau_f)\eta_0, \tag{4}$$

$$\mu_+ = \mu_- = (1 - x_r)\mu_0. \tag{5}$$

The nominal values η_0 and μ_0 are chosen following the design guidelines presented in [16], whereas the mode transition signal x_r is generated by appending a ramp-down to the trailing edge of fault signal x_f as shown in Fig. 3. The ramp-down over a short period t_F ensures smooth transition at fault clearing.

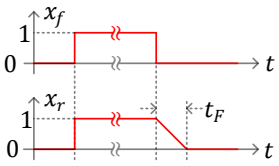

Figure 3. The mode transition signal x_r is generated from the fault signal x_f.

The implementations of the positive and negative sequence SVOs are shown in Fig. 4.

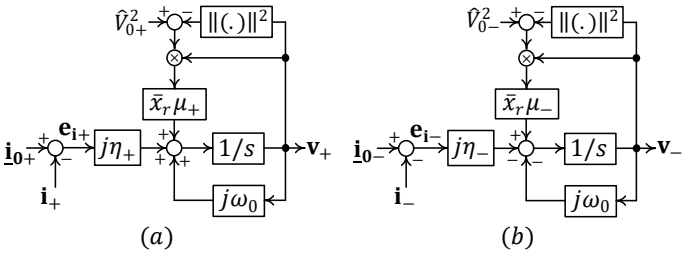

Figure 4. Implementation of synchronizing units - (a) positive-sequence SVO, (b) negative-sequence SVO.

The principle of operation of the two SVOs through power synchronization is presented in Section IV.

B. Double-Sequence Current Reference Generation

For a given set of real and reactive power references, the current references are generated using the controller internal states $\mathbf{v}_+$ and $\mathbf{v}_-$. In [16], current references are generated using instantaneous power theory. However, for asymmetric operation the coupling between the power flows in the two sequences substantially complicates the current reference generation. Various current reference generation methods have been proposed for asymmetrical FRT in GFL converters [19]–[21], [28]. For flexibility in control capability such as balanced current injection, constant real power flow, and positive and negative sequence reactive power compensation, the reference generation method reported in [20], [21] is adopted in this work. The sequence current references $\mathbf{i_{0+}} = i_{\alpha 0+} + ji_{\beta 0+}$ and $\mathbf{i_{0-}} = i_{\alpha 0-} + ji_{\beta 0-}$ are generated as

$$\begin{aligned} \mathbf{i}_{\alpha\mathbf{0}+} &= \frac{2}{3}\left\{\frac{k_{p+}v_{\alpha+}}{D_p}P_0 + \frac{k_{q+}v_{\beta+}}{D_q}Q_0\right\}, \\ \mathbf{i}_{\beta\mathbf{0}+} &= \frac{2}{3}\left\{\frac{k_{p+}v_{\beta+}}{D_p}P_0 - \frac{k_{q+}v_{\alpha+}}{D_q}Q_0\right\}, \\ \mathbf{i}_{\alpha\mathbf{0}-} &= \frac{2}{3}\left\{\frac{k_{p-}v_{\alpha-}}{D_p}P_0 + \frac{k_{q-}v_{\beta-}}{D_q}Q_0\right\}, \\ \mathbf{i}_{\beta\mathbf{0}-} &= \frac{2}{3}\left\{\frac{k_{p-}v_{\beta-}}{D_p}P_0 - \frac{k_{q-}v_{\alpha-}}{D_q}Q_0\right\}, \end{aligned} \tag{6}$$

where $D_p = k_{p+}\|\mathbf{v}_+\|^2 + k_{p-}\|\mathbf{v}_-\|^2$ and $D_q = k_{q+}\|\mathbf{v}_+\|^2 + k_{q-}\|\mathbf{v}_-\|^2$. Desired control objective can be obtained with proper selection of k_{p+}, k_{p-}, k_{q+}, and k_{q-} [21].

C. Double Sequence Vector Limiter

To prevent over-current at the converter output under fault conditions, the current reference vector must be limited below the maximum value allowable by the converter hardware. A circular limiter used in [16], [17] cannot be used on asymmetric set of current references.

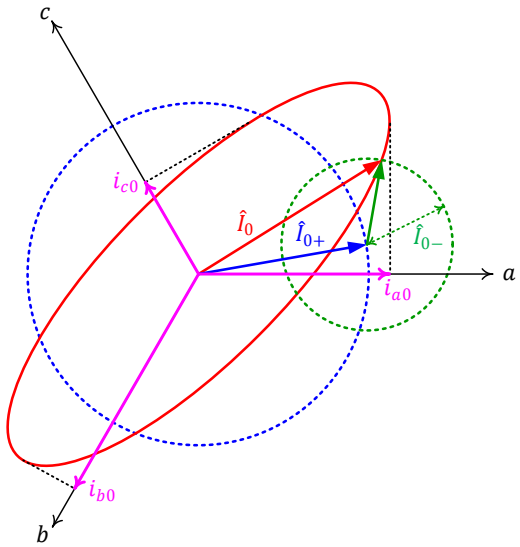

Figure 5. Asymmetric current vector follows an elliptical trajectory.

Fig. 5 illustrates the positive-sequence component $\mathbf{i_{0+}}$ and negative-sequence component $\mathbf{i_{0-}}$ of an arbitrary set of asymmetric current reference vector $\mathbf{i_0}$. The instantaneous sum of the two inversely rotating vectors $\mathbf{i_{0+}}$ and $\mathbf{i_{0-}}$, results in an elliptical trajectory of the total current vector $\mathbf{i_0}$. For over-current limiting below the maximum value $\hat{I}_m$ allowable by the converter hardware, the current reference is to be saturated as

$$\underline{i}_0 = \{[\underline{i}_{a0}\ \underline{i}_{b0}\ \underline{i}_{c0}]^T \ : \ \max\{|\underline{i}_{a0}|, |\underline{i}_{b0}|, |\underline{i}_{c0}|\} \le \hat{I}_m\}, \tag{7}$$

First, the instantaneous magnitudes of the three-phase unsaturated current references are obtained as

$$i_{a0/b0/c0} = \{\|\mathbf{i_{0+}}\|^2 + \|\mathbf{i_{0-}}\|^2 + 2(\xi_1 \cos 2\gamma - \xi_2 \sin 2\gamma)\}^{1/2}, \tag{8}$$

where $\xi_1 = 2(i_{\alpha 0+}i_{\alpha 0-} - i_{\beta 0+}i_{\beta 0-})$ and $\xi_2 = 2(i_{\beta 0+}i_{\alpha 0-} + i_{\alpha 0+}i_{\beta 0-})$ and

$$\gamma = \begin{cases} 0, & \text{for phase a} \\ -2\pi/3, & \text{for phase b} \\ 2\pi/3, & \text{for phase c.} \end{cases} \tag{9}$$

Next, the saturated current references are obtained as

$$\begin{aligned} \mathbf{i_{0+}} = k_{sat}\mathbf{i_{0+}}; \quad \mathbf{i_{0-}} = k_{sat}\mathbf{i_{0-}} \\ k_{sat} = \frac{\hat{I}_m}{\max\{|i_{a0}|, |i_{b0}|, |i_{c0}|\}} \end{aligned} \tag{10}$$

The active resistance R_0 (see Fig. 2) is used for fast over-current limiting under fault condition. The various parts of the virtual impedance $Z_v(s)$ are implemented as

$$Z_v(s) = \frac{R_v}{s/\omega_b + 1} + x_r\frac{L_v}{s/\omega_b + 1} + \sum_h Z_h(s), \tag{11}$$

where virtual resistance R_v can be used for augmenting system damping and the virtual inductance L_v can be used for fast over-current limiting at the fault instant [16], [17]; resonant filters $\sum_h Z_h(s)$ can be added for harmonic current suppression [14]. Note that the complete controller shown in Fig. 2 is used under both nominal and fault conditions. As explained in Section IV-B, under normal operating condition with a symmetric grid voltage, the controller inherently achieves $\mathbf{i_{0-}} = 0$ and $\mathbf{i_{-}} = 0$.

The level of voltage unbalance at the PoC is characterized by the unbalance factor (UF), defined as UF=$\|\mathbf{v_{g-}}\|/\|\mathbf{v_{g+}}\|$. A fault signal is latched, i.e., $x_f = 1$, once an over-current is detected as $|i_x| > \hat{I}_{Tf}, \forall x \in \{a, b, c\}$ in any of the phases or a voltage unbalance above a threshold K_{UTf} is detected as UF$> K_{UTf}$. The fault is cleared, i.e., $x_f = 0$, once the positive-sequence voltage returns to the nominal range as $\|v_+\| > \hat{V}_{Tc}$ and the UF falls below the clearing threshold $< K_{UTc}$.

IV. Principle of Synchronization

The proposed dsUVOC utilizes power synchronization through transient transfer of power in both positive- and negative-sequences. For ease of explanation, the double-sequence vector limiter on the current reference is excluded and the virtual impedance is lumped together with the source/-grid impedance. We consider the simplified system with an arbitrary operating point, shown in Fig. 6, for the analysis presented in Sections IV-A and IV-B; furthermore, power synchronization in each sequence is analyzed separately since the complicated coupled dynamics in the two sequences offer little physical insight.

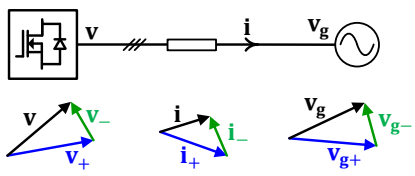

Figure 6. Simplified system for analysis of the double-sequence power synchronization.

A. Positive-Sequence Synchronization

To illustrate the positive-sequence synchronization mechanism, we consider $k_{p+} = 1$, $k_{p-} = 0$, $k_{q+} = 1$, $k_{q-} = 0$ and the negative-sequence SVO is excluded. Following similar steps used in [16], (1) can be rearranged as

$$\dot{\mathbf{v}}_+ = [j(\omega_0 + \eta_+ e_{iP+}) + (\mu_+ e_{v+} - \eta_+ e_{iQ+})]\mathbf{v}_+, \tag{12}$$

where

$$\begin{aligned} e_{iP+} = \frac{2(P_{0+} - P_+)}{3\|\mathbf{v}_+\|^2}; \quad e_{iQ+} = \frac{-2(Q_{0+} - Q_+)}{3\|\mathbf{v}_+\|^2}, \\ P_+ + jQ_+ = \mathbf{v}_+\mathbf{i}'_+; \quad P_{0+} + jQ_{0+} = \mathbf{v}_+\mathbf{i}'_{\mathbf{0+}}, \\ e_{v+} = \hat{V}_{0+}^2 - \|\mathbf{v}_+\|^2, \end{aligned} \tag{13}$$

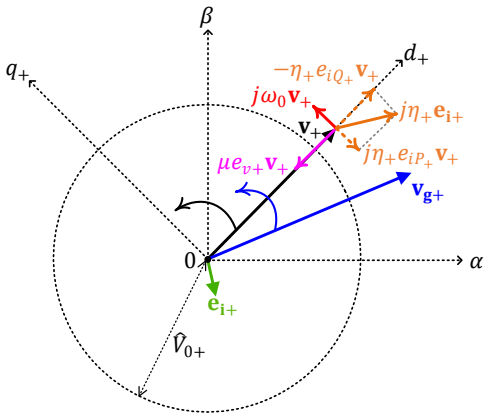

Figure 7. Power synchronization of the positive-sequence SVO.

and $(.)'$ denotes complex-conjugate of the respective complex vector. Now, we consider a synchronous reference frame aligned with the positive-sequence SVO output voltage vector $\mathbf{v}_+$. For an arbitrary positive-sequence source/grid voltage vector $\mathbf{v_g}+$ and a current error $\mathbf{e_{i+}} = \mathbf{i_{0+}} - \mathbf{i}_+$, a graphical representation of the SVO dynamics given by (12) is shown in Fig. 7, where the α and β axes mark the stationary reference frame. Note that the real and imaginary parts of the complex coefficient of $\mathbf{v}_+$ in (12) denote the instantaneous frequency ω_+ and normalized rate of change of the instantaneous vector magnitude $(1/V_+)d(V_+)/dt$, respectively [16], where $V_+ = \|\mathbf{v}_+\|/\sqrt{(2)}$. Evidently, instantaneous droop responses such as P_+ vs. ω and Q_+ vs. $\|\mathbf{v}\|^2$ are observed on the SVO output voltage vector along the synchronous d_+ and q_+ axes, respectively as

$$\begin{aligned} \omega_+ = \dot{\delta}_+ = \omega_0 + \frac{\eta_+}{3V_+^2}(P_{0+} - P_+), \\ \dot{V}_+ = 2\mu_+ V_+(V_{0+}^2 - V_+^2) + \frac{\eta_+}{3V_+}(Q_{0+} - Q_+), \end{aligned} \tag{14}$$

which facilitate the power synchronization to the positive-sequence grid voltage vector $\mathbf{v_g}+$. The droop responses under current constrained operation can be derived as

$$\begin{aligned} \omega_+ = \dot{\delta}_+ = \omega_0 + \frac{\eta_+}{3V_+^2}\left(k_{sat}P_{0+} - P_+\right), \\ \dot{V}_+ = \frac{\eta_+}{3V_+^2}\left(k_{sat}Q_{0+} - Q_+\right). \end{aligned} \tag{15}$$

Evidently, power synchronization mechanism is retained as the $P_+ - \omega_+$ dynamics remains unaltered; only the power references are scaled proportionately with the voltage magnitude.

B. Negative-Sequence Synchronization

Excluding the positive-sequence SVO and taking $k_{p+} = 0$, $k_{p-} = 1$, $k_{q+} = 0$, $k_{q-} = 1$ and following similar notations as those used in the preceding subsection IV-A, the negative-sequence SVO dynamics in (1) can be rearranged as

$$\dot{\mathbf{v}}_- = [-j(\omega_0 + \eta_- e_{iP-}) + (\mu_- e_{v-} - \eta_- e_{iQ-})]\mathbf{v}_-. \quad (16)$$

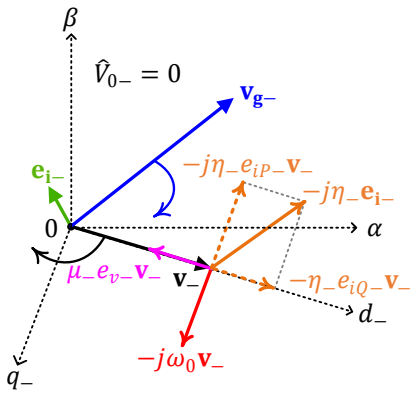

Figure 8. Power synchronization of the negative-sequence SVO.

For an arbitrary negative-sequence source/grid voltage vector $\mathbf{v_g}-$ and an current error $\mathbf{e_{i-}} = \mathbf{i_{0-}} - \mathbf{i}_-$, a graphical representation of the SVO dynamics in the negative-sequence synchronous frame aligned with $\mathbf{v}_-$is shown in Fig. 8. Evidently, instantaneous droop responses such as P_- vs. ω and Q_- vs. $\|\mathbf{v}_-\|^2$, similar to those in the positive-sequence, are also obtained along the d_- and q_- axes, respectively. Consequently, instantaneous droop responses in the negative-sequence are achieved as

$$\begin{aligned} \omega_- &= \dot{\delta}_- = \omega_0 + \frac{\eta_-}{3V_-^2}(P_{0-} - P_-), \\ \dot{V}_- &= 2\mu_- V_-(V_{0-}^2 - V_-^2) + \frac{\eta_-}{3V_-}(Q_{0-} - Q_-). \end{aligned} \quad (17)$$

This enables power synchronization to the negative-sequence grid voltage vector $\mathbf{v_{g-}}$. Droop responses under current constrained operation similar to (15) can be derived for negative sequence also. Note that the negative-sequence voltage reference is set as $\hat{V}_{0-} = 0$ and under normal operation the power references as chosen as $P_{0-} = 0$ and $Q_{0-} = 0$ which leads to $\mathbf{i_{0-}} = 0$; for a balanced grid, $\mathbf{v_{g-}} = 0$ which results in $\mathbf{v}_- = 0$ and $\mathbf{i}_- = 0$.

C. Double-Sequence Synchronization

The current reference generation given by (6) uses total power references P_0 and Q_0 and results in sequence power references as

$$\frac{P_{0-}}{P_{0+}} = \frac{k_{p-}\|\mathbf{v}_-\|}{k_{p+}\|\mathbf{v}_+\|}; \quad \frac{Q_{0-}}{Q_{0+}} = \frac{k_{q-}\|\mathbf{v}_-\|}{k_{q+}\|\mathbf{v}_+\|}, \quad (18)$$

where $k_{p-} = 0$ and $k_{q-} = 0$ lead to $P_{0-} = 0$ and $Q_{0-} = 0$, respectively. Symmetric and asymmetric faults can be distinguished by the voltage unbalance factor (UF). Under symmetric faults, $k_{p-} = 0$ and $k_{q-} = 0$ are used since negative-sequence compensation is not required. Now, using the full form of the current reference generation given by (6) and considering current constrained operation, the positive- and negative-sequence droop responses can be derived as

$$\begin{aligned} \omega_+ &= \omega_0 + \frac{\eta_+}{3V_+^2}\left(\frac{2k_{p+}V_+^2}{D_p}k_{sat}P_0 - P_+\right), \\ \dot{V}_+ &= 2\mu_+ V_+(V_{0+}^2 - V_+^2) + \frac{\eta_+}{3V_+}\left(\frac{2k_{q+}V_+^2}{D_q}k_{sat}Q_0 - Q_+\right), \\ \omega_- &= \omega_0 + \frac{\eta_-}{3V_-^2}\left(\frac{2k_{p-}V_-^2}{D_p}k_{sat}P_0 - P_-\right), \\ V_-^2 &= 2\mu_- V_-(V_{0-}^2 - V_-^2) + \frac{\eta_-}{3V_-}\left(\frac{2k_{q-}V_-^2}{D_q}k_{sat}Q_0 - Q_-\right). \end{aligned} \quad (19)$$

Evidently, the $P_+ - \omega_+$ and the $P_- - \omega_-$ droop responses are unaffected and the coupling among the two sequences exists only through the power references. This enables the simultaneous double synchronous operation of the proposed controller.

V. Experimental Results

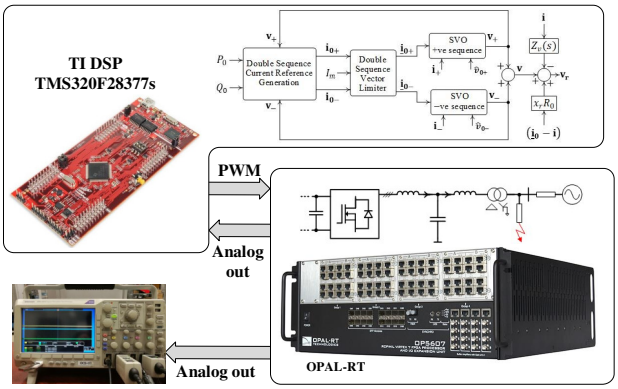

Figure 9. Real-time control hardware-in-the-loop (CHIL) test setup.

Table I
Voltage Source Converter Ratings

Symbol	Parameter	Value
S_{rated}	Rated power	10.8 kVA
P_{rated}	Rated real power	9 kW
Q_{rated}	Rated reactive power	6 kVAR
V_0	Nom. (L-N RMS) voltage	120 V
ω_0	Nom. frequency	$2\pi(60)$ rad/s
f_{sw}	Switching frequency	10 kHz
f_s	Sampling frequency	20 kHz
L_1	Converter-side inductor	≈ 0.046 pu
L_2	Network-side inductor	≈ 0.058 pu
C_f	Filter capacitor	≈ 0.036 pu

Table II
CONTROLLER PARAMETERS

η_0	16.63
μ_0	7.1×10^{-4}
τ_f	0.07
R_0	0.52 pu
L_v	0.2 pu ($Z_{xer} = 0.1$) pu
L_v	0.008 pu ($Z_{xer} = 0.5$ pu)
R_v	0.002 pu
ω_b	$2\pi(200)$ rad/s
I_m	1.2 pu

A controller hardware-in-the-loop (CHIL) test bed is set up to validate the proposed controller. The test setup is shown in Fig. 9. The VSC system including the feeder transformer and the grid are modeled in real-time OPAL-RT platform. The proposed dsUVOC is implemented using Texas Instruments' C2000 digital signal processor *TMS320F28377s*. The VSC ratings and the controller parameters are listed in Table I and Table II, respectively. The control parameters are selected following the design guidelines provided in [16]. The grid and fault impedances are set as $Z_g = 0.019$ pu and $Z_f = 0.019\%$ pu, respectively, with reactance to resistance ratio of $X/R = 20$. To evaluate the controller performance under different feeder strength at the PoC, we consider three different impedance values of the Δ-Yg transformer as $Z_{xer} = 0.1$ pu and 0.5 pu. Note that the VSC ratings (V_0 and P_{rated}) are used as the base quantities for the pu notation. Therefore, the different values of Z_{xer} emulate different source strengths, i.e., SCR while looking into the PoC from the VSC side.

A. Single-Line-to-Ground Fault

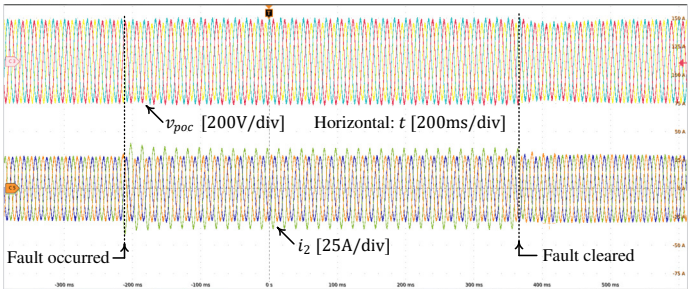

Figure 10. FRT response to a SLG fault for $Z_{xer} = 0.5$pu.

Fig. 10 shows the ride-through response to a SLG fault for a weak source/feeder condition. At pre-fault condition the power references are set as $P_0 = 0.75$ pu and $Q_0 = 0$. Once the fault is detected, the reactive power reference is set as $Q_0 = (S_{rated}^2 - P_0^2)^{1/2}$. The test data is further analyzed to evaluate the positive- and negative-sequence voltage and current magnitudes, and the UF at the PoC, which are shown in Fig. 11. Note that the converter output current is limited below the maximum allowable value $\hat{I}_m$. The positive-sequence voltage is boosted up as well as the UF, marked in red in Fig. 11, is improved/lowered compared to the uncompensated UF (marked by blue dashed line). The uncompensated UF is

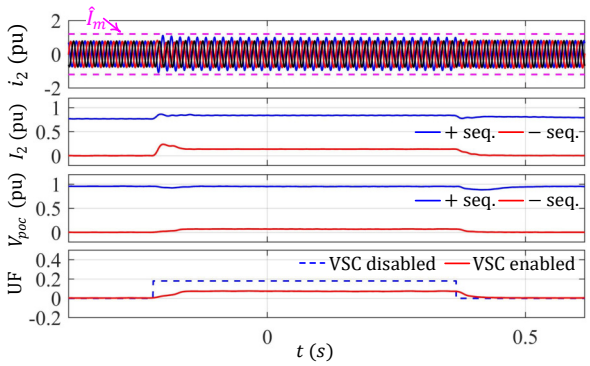

Figure 11. Analysis of test data for SLG fault for $Z_{xer} = 0.5$pu (Fig. 10).

measured at the PoC separately under identical fault condition when the VSC is disabled. Once the fault is cleared, normal operation is quickly restored.

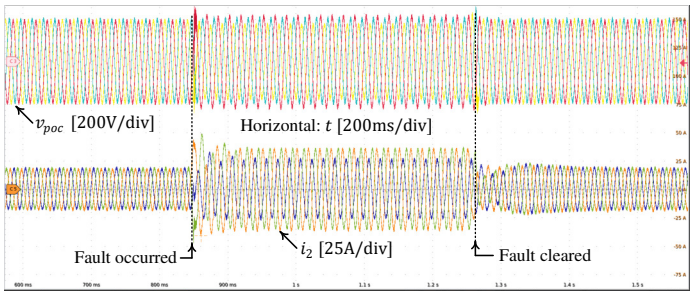

Figure 12. FRT response to a SLG fault for $Z_{xer} = 0.1$pu.

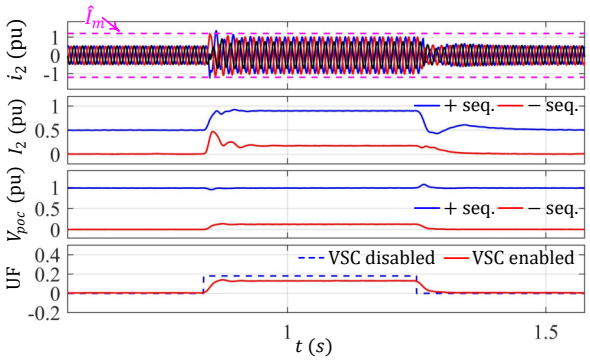

Figure 13. Analysis of test data for SLG fault for $Z_{xer} = 0.1$ pu (Fig. 12).

Next the experiment is repeated under a strong source/feeder condition with $Z_{xer} = 0.1$ pu and the corresponding results and data analysis are shown in Fig. 12 and Fig. 13, respectively. The output current is quickly limited below $\hat{I}_m$ and the positive-sequence voltage at the PoC is restored under fault, whereas the negative-sequence voltage is lowered to improve the UF compared to the uncompensated UF under fault.

B. Double-Line-to-Ground (DLG) Fault

FRT response and the corresponding data analysis under a weak source/feeder condition ($Z_{xer} = 0.5$ pu) are shown in Fig. 14 and Fig. 15, respectively.

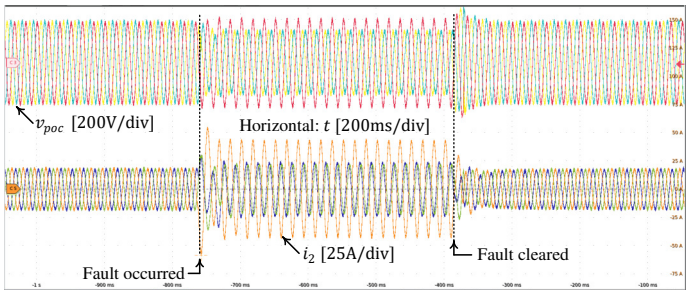

Figure 14. FRT response to a DLG fault for $Z_{xer} = 0.5$pu.

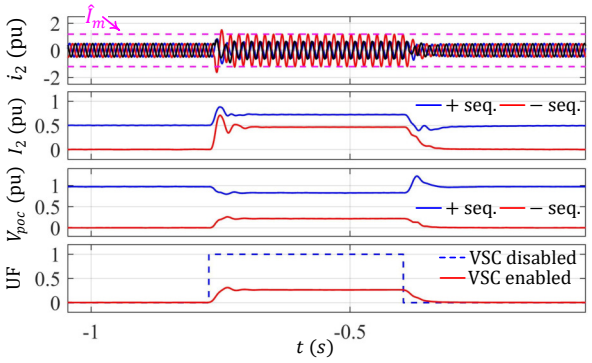

Figure 15. Analysis of test data for DLG fault for $Z_{xer} = 0.5$ pu (Fig. 14).

From the uncompensated UF, it is evident that the DLG leads to severe voltage unbalance at the PoC which results in momentary rise in the converter output current; however, the converter quickly limits the output current at the maximum allowable value $\hat{I}_m$. Leveraging the full current capability (current saturated operation), the controller substantially improves the voltage UF at the PoC. Normal operation is restored quickly without any noticeable transients in the output current once the fault is cleared.

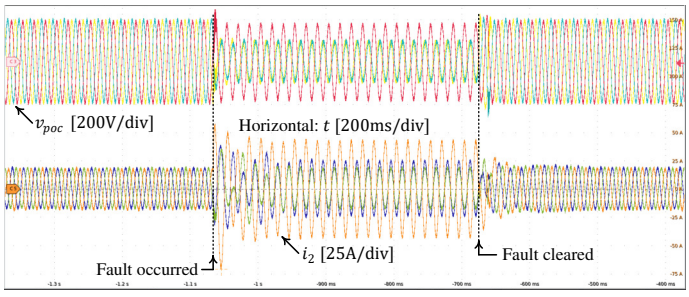

Figure 16. FRT response to a DLG fault for $Z_{xer} = 0.1$pu.

Next the test is repeated under a strong source/feeder condition with $Z_{xer} = 0.1$ and the corresponding results are shown in Fig. 16 and Fig. 17, respectively. Due to the lower source impedance compared to that in the weak-source case (Fig. 15), a higher initial overshoot in converter output current is observed at the fault instant. The controller quickly limits the current at $\hat{I}_m$ while lowering the PoC voltage UF. Note that the lower feeder impedance results in a lower improvement in the UF relative to Fig. 15 for the given current capability of the converter hardware.

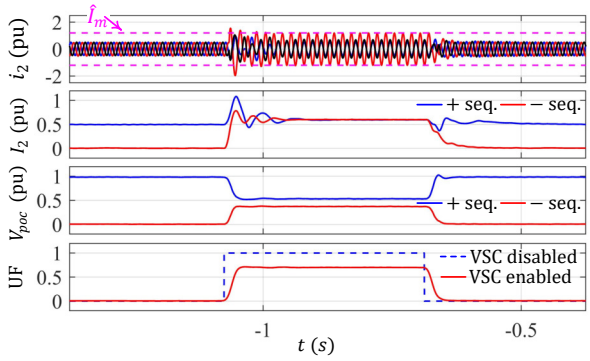

Figure 17. Analysis of test data for DLG fault for $Z_{xer} = 0.1$ pu (Fig. 16).

VI. Conclusion

The proposed dsUVOC leverages simultaneous power synchronization in both positive- and negative-sequences, which enables synchronization to balanced, distorted, or unbalanced grids. Through sequence-decoupled as well as positive- and negative-sequence coupled space vector analysis, double-sequence power synchronization has been illustrated. This enhanced synchronization capability, combined with fast overcurrent limiting, facilitates ride-through of both symmetric and asymmetric faults. The proposed controller has been validated through real-time CHIL experiments.

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