Novel Bidirectional Universal 1-Phase/3-Phase-Input Unity Power Factor Differential AC/DC Converter

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A common 400 V dc bus for industrial motor drives advantageously allows the use of high-performance 600 V power semiconductor technology in the inverter drive converter stages and to lower the rated power of the supplying rectifier system. Ideally, this supplying rectifier system features unity power factor operation, bidirectional power flow and nominal power operation in the three-phase *and* the single-phase grid. This paper introduces a novel bidirectional universal single-/three-phase-input unity power factor differential ac-dc converter suitable for the above mentioned requirements: The basic operating principle and conduction states of the proposed topology are derived and discussed in detail. Then, the main power component voltage and current stresses are determined and simulation results in PLECS are provided. The concept is verified by means of experimental measurements conducted in both three-phase *and* single-phase operation with a 6 kW prototype system employing a switching frequency of 100 kHz and 1200 V SiC power semiconductors.

Introduction: A local dc distribution system [1, 2, 3, 4, 5, 6, 7, 8] , i.e., several dc loads connected to a common dc bus which is supplied from the ac grid by a bidirectional Power Factor Correction (PFC) rectifier, advantageously decreases the realization effort compared to a solution where each dc load is supplied by an individual PFC rectifier. Further, regenerative loads can partially cover the power demands of other dc loads without loading the PFC rectifier (thus reducing conversion losses) and a local energy storage enables peak load shaving with an additional reduction of the peak grid power demand.

Typical examples of such local dc distribution systems are industrial automation and robotics where several Variable Speed Drives (VSDs) are connected to a common dc bus voltage. There, a dc-bus voltage of $U_{\rm dc} = 400\,{\rm V}$ allows the use of high-performance and cost-effective 600 V wide-bandgap power semiconductors in the VSD inverter stages [9]. In case the common dc bus is supplied from the European single-phase grid (line-to-neutral voltage $U_{\rm ac} = 230\,{\rm V_{RMS}}/\hat{U}_{\rm ac} = 325\,{\rm V_{pk}}$) a boost-type PFC rectifier generates the desired $U_{\rm dc} = 400\,{\rm V}$ [10]. In contrast, if the 400 V dc bus is supplied with higher power levels from the European three-phase grid a buck-type PFC rectifier is required (a boost-type system is limited to dc voltages above the line-to-line voltage $\sqrt{3}\cdot\hat{U}_{\rm ac}$ [10] with typically $U_{\rm dc} = 680...800\,{\rm V}$) such that two different PFC rectifier systems are employed today depending on the considered single-phase or three-phase grid input.

Considering economies of scale, next generation PFC rectifiers for the supply of 400 V dc distribution systems feature nominal power operation in both a three-phase *and* a single-phase grid. This paper proposes the new PFC rectifier topology presented in **Fig. 1** which advantageously shows identical stresses of the main power components in single- *and* three-phase operation, such that nominal power delivery is possible independent of the available number of grid phases. The paper is structured as follows: First, the derivation of the topology, the basic operating behavior, and the voltage and current stress of the main power component is introduced. Then, simulation results for single- and three-phase operation are provided, and experimental results validating the converter concept based on a 6 kW prototype system are presented. Last, the findings and key contributions of the paper are summarized.

Proposed topology operating behavior: The proposed differential rectifier is based on the phase-modular buck-boost Y-rectifier [11, 12] and comprises three identical input stages, each one comprising a buck-boost dc-dc converter structure connected to a common star "Y" point given by the negative dc output rail n. In case of three-phase operation (**Fig. 1a**), grid phase voltages $u_{\rm a}$,$u_{\rm b}$,$u_{\rm c}$ (with amplitude $\hat{U}_{\rm ac}$) are connected to the ac-side terminals a, b, and c, respectively, and the converter realizes sinusoidal grid currents $i_{\rm a}$,$i_{\rm b}$,$i_{\rm c}$ (with amplitude $\hat{I}_{\rm ac}$) in phase with the respective grid voltages. In contrast to the standard Y-rectifier, for the proposed topology the positive terminal p of the dc output voltage is referenced to the grid neutral point N (highlighted in orange in (**Fig. 1**), resulting in a phase module structure similar to the grid-side converter stage of [13]. In case of single-phase operation (**Fig. 1b**), the grid voltage $u_{\rm a}$ is connected to the parallel-connected ac-side terminals a, b, and c

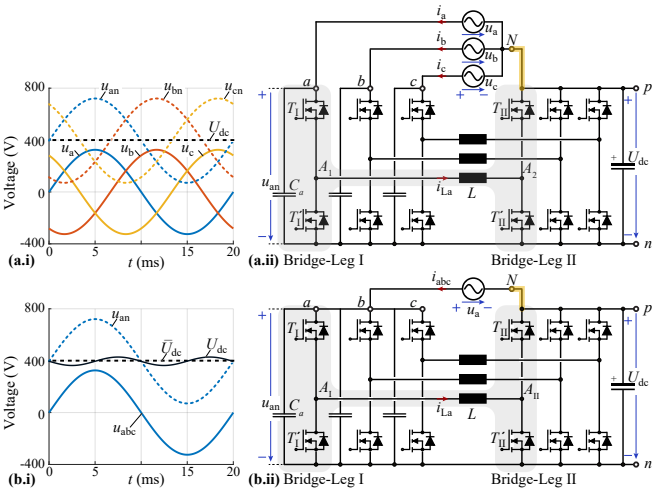

Fig. 1 *Main circuit structure and input-output terminal voltage waveforms of the proposed bidirectional differential single-/three-phase input Y-rectifier in three-phase (**a**) and single-phase operation (**b**); the phase module a is highlighted in light gray.*
a.i grid voltages $u_{\rm a}$,$u_{\rm b}$,$u_{\rm c}$, input / ac-stage capacitor voltages $u_{\rm an}$,$u_{\rm bn}$,$u_{\rm cn}$ and dc output voltage $U_{\rm dc}$ for three-phase operation;
a.ii main power circuit structure for three-phase operation.
b.i grid voltages $u_{\rm a}$, input / ac-stage capacitor voltage $u_{\rm an}$, and dc output voltage $U_{\rm dc}$ for single-phase operation (note that $U_{\rm dc}$ comprises the characteristic twice-mains-frequency voltage fluctuation on top of its average value $\bar{U}_{\rm dc}$);
b.ii main power circuit structure for single-phase operation.

such that the grid current $i_{\rm abc}$ is evenly shared between the phase modules with $i_{\rm a} = i_{\rm b} = i_{\rm c} = \frac{1}{3} i_{\rm abc}$, and the connection of the grid neutral point N and the positive dc output voltage terminal p creates a return path for the single-phase grid current $i_{\rm abc}$.

The basic operating concept is identical for all phase modules a,b,c and is hence only explained for phase module a which is highlighted in **Fig. 1**. The phase power $P_{\rm a} = \frac{1}{2}\hat{U}_{\rm ac}\hat{I}_{\rm ac}$ (equal to $\frac{1}{3}$ of the total input power $P_{\rm abc}$) is processed by two half-bridges $A_{\rm I}$ and $A_{\rm II}$ which are connected via the inductor L. The input capacitor C_a (serving filtering and commutation purposes) is placed in the half-bridge $A_{\rm I}$, whose time-domain voltage is according to Kirchhoff's voltage law

$$u_{\rm an}(t) = u_{\rm a}(t) + U_{\rm dc}, \tag{1}$$

as highlighted in **Fig. 1a.i** and **b.i** for three-phase and single-phase operation, respectively. To prevent short-circuit via the anti-parallel diodes of the power switches $T_{\rm I}$ and $T'_{\rm I}$ the input stage voltage $u_{\rm an}$ has to be strictly positive and ac operation of the phase module is enabled by the *differential* interaction of the positive voltages $u_{\rm an}$ and $U_{\rm dc}$ (accordingly, the system is named *differential* rectifier [14]). The requirement of $u_{\rm an} > 0$ and (1) constrain the dc output voltage to values above the grid line-to-neutral amplitude, i.e.,

$$U_{\rm dc} > \hat{U}_{\rm ac}, \tag{2}$$

which corresponds to the operating limit of a standard boost-type single-phase PFC rectifier and represents a limitation compared to the standard Y-rectifier which can generate any $U_{\rm dc} > 0$. Note that (2) applies here to both single- and three-phase operation of the proposed converter and is compatible with the considered $U_{\rm dc} = 400\,{\rm V}$ and $\hat{U}_{\rm ac} = 325\,{\rm V_{pk}}$ of the European grid.

The conduction states of the power semiconductor $T_{\rm I}/T'_{\rm I}$ and $T_{\rm II}/T'_{\rm II}$ are highlighted in **Fig. 2**. When the mains voltage is positive, $u_{\rm a} > 0$ (see **Fig. 2a**), the converter operates in mode I where only the half-bridge $A_{\rm I}$ is switched, while the upper-side transistor of $A_{\rm II}$, $T_{\rm II}$, is continuously activated. This mode I corresponds to buck-boost operation with discontinuous power flow from the grid $u_{\rm a}$ to the dc voltage $U_{\rm dc}$. Conversely, when the mains voltage is negative, $u_{\rm a} < 0$ (see **Fig. 2b**), the converter operates in mode II, and only the half-bride $A_{\rm II}$ is switched, with the upper-side transistor of the opposite branch, $T_{\rm I}$, continuously activated. This mode II corresponds to a step-up or boost operation with $|u_{\rm a}(t)| < U_{\rm dc}$.

Assuming that the switching frequency $f_{\rm s}$ is much higher than the mains frequency $f_{\rm ac}$, the duty cycles $d_{\rm AI}$ and $d_{\rm AII}$, which define the

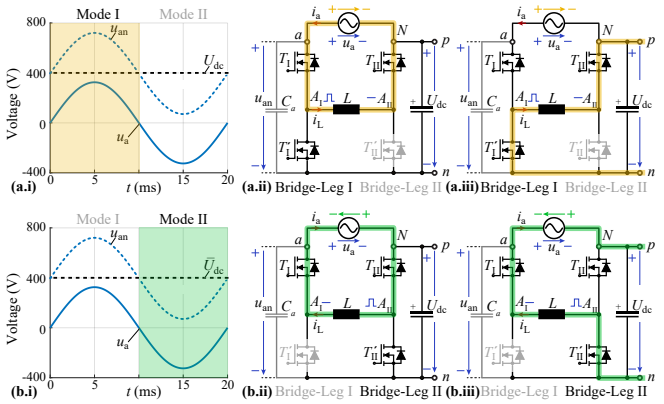

Fig. 2 *Conduction states of the phase module a of the proposed converter structure in (**a**) mode I and (**b**) mode II (note that the grid voltage u_a represents the first filter stage capacitor of a real converter realization; also, the input/commutation capacitor C_a is assumed to be small such that it does not represent a relevant high-frequency current path).*

a.i terminal voltage waveforms (grid voltage u_a, module input capacitor voltage u_an and dc output voltage U_dc) with highlighted mode I operating region where $u_\mathrm{an} > U_\mathrm{dc}$;
a.ii mode I conduction state 1 (the inductor L is magnetized by the instantaneously positive grid voltage u_a);
a.iii mode I conduction state 2 (the inductor L is demagnetized by the dc output voltage U_dc).
b.i terminal voltage waveforms with highlighted mode II operating region where $u_\mathrm{an} \leq U_\mathrm{dc}$;
b.ii mode II conduction state 1 (the inductor L is magnetized by the instantaneously negative grid voltage u_a);
b.iii mode II conduction state 2 (the inductor L is demagnetized by the difference of the grid voltage u_a and dc output voltage U_dc).

high-side switches activation of half-bridges A_I and A_II, respectively, are obtained as follows

$$d_\mathrm{AI}(t) = \begin{cases} \frac{U_\mathrm{dc}}{U_\mathrm{dc}+u_\mathrm{a}(t)}, & u_\mathrm{a} \geq 0 \\ 1, & u_\mathrm{a} < 0 \end{cases}, \tag{3}$$

$$d_\mathrm{AII}(t) = \begin{cases} 1, & u_\mathrm{a} \geq 0 \\ \frac{U_\mathrm{dc}+u_\mathrm{a}(t)}{U_\mathrm{dc}}, & u_\mathrm{a} < 0 \end{cases}. \tag{4}$$

Neglecting the low-frequency input capacitor C_a current, the local average current in a switching period $T_\mathrm{s} = 1/f_\mathrm{s}$ through the inductor $\langle i_\mathrm{La} \rangle$ can be expressed as follows

$$\langle i_\mathrm{La} \rangle(t) = \begin{cases} (1 + \frac{u_\mathrm{a}(t)}{U_\mathrm{dc}}) i_\mathrm{a}(t) = \frac{i_\mathrm{a}(t)}{d_\mathrm{AI}(t)}, & u_\mathrm{a} \geq 0 \\ i_\mathrm{a}(t), & u_\mathrm{a} < 0 \end{cases}. \tag{5}$$

Therefore, assuming lossless and unity power factor operation, for a phase power $P_\mathrm{a} = U_\mathrm{ac} I_\mathrm{ac}$, the low frequency RMS component of the inductor current flowing through the half-bridge branches can be expressed as

$$\langle I_\mathrm{La} \rangle_\mathrm{RMS} = \frac{I_\mathrm{ac}}{U_\mathrm{dc}} \sqrt{U_\mathrm{dc}^2 + \frac{3}{4} U_\mathrm{ac}^2 + \frac{8\sqrt{2}}{3\pi} U_\mathrm{dc} U_\mathrm{ac}}, \tag{6}$$

and is elevated by approximately 40 % compared to the grid RMS current I_ac for the considered $U_\mathrm{ac} = 230\,\mathrm{V_{RMS}}$ and $U_\mathrm{dc} = 400\,\mathrm{V}$. Note that $\langle I_\mathrm{La} \rangle_\mathrm{RMS}$ is identical in both three-phase and single-phase operation for a given power and grid voltage level.

An other important converter metric is given by the required semiconductor blocking voltage. For the ac-stage A_1 the maximum voltage is defined by $U_\mathrm{an,max} = U_\mathrm{dc} + \hat{U}_\mathrm{ac} = 725\,\mathrm{V}$ which hence requires 1200 V power semiconductors to ensure sufficient blocking voltage margin during switching transients (alternatively, the three-level flying capacitor ac-stage structure from [15] would allow the use of high-performance and cost-effective 600 V semiconductors). In contrast, the voltage stress in the dc-side half-bridge A_II branch is equal to the converter output voltage, $U_\mathrm{dc} = 400\,\mathrm{V}$, such that 600 V semiconductors can be employed. An important result and benefit of the proposed topology is that also equal voltage stress results in both three-phase and single-phase operation provided that the line-to-neutral (RMS) voltage U_ac is the same.

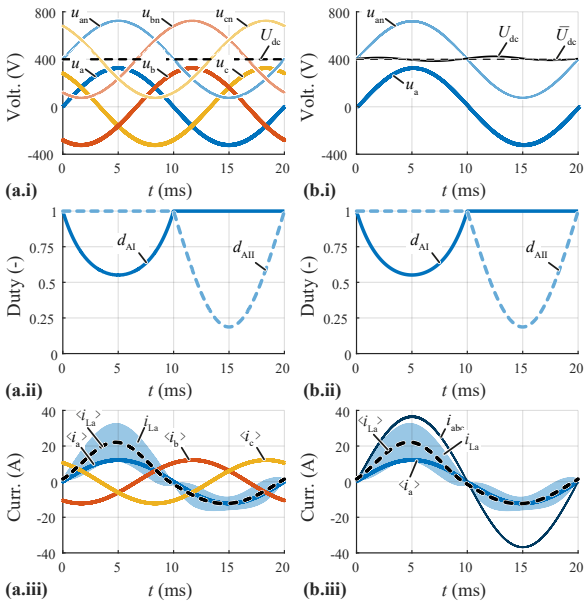

Fig. 3 *Simulated waveforms in open-loop modulation with an output power of 6 kW in three-phase (**a**) and single-phase operation (**b**).*

x.i grid voltages u_a,u_b,u_c and phase a grid current i_a;
x.ii phase a buck-stage d_{A_1} and boost-stage duty cycle d_{A_2};
x.iii low-frequency grid currents $\langle i_\mathrm{a} \rangle$,$\langle i_\mathrm{b} \rangle$,$\langle i_\mathrm{c} \rangle$ and phase a inductor current i_La (with the local-average value within one switching period $\langle i_\mathrm{La} \rangle$ highlighted on top with a dashed line) and grid current $\langle i_\mathrm{a} \rangle$.

Simulation Results: The main simulation results of the proposed topology (specifications according to **Tab. 1**) using PLECS for $U_\mathrm{ac} = 230\,\mathrm{V_{RMS}}$ / $f_\mathrm{ac} = 50\,\mathrm{Hz}$, an output voltage $U_\mathrm{dc} = 400\,\mathrm{V}$, and a power level $P_\mathrm{abc} = 3 \times P_\mathrm{a} = 6\,\mathrm{kW}$ are presented in **Fig. 3** for three-phase (**a**) and single-phase (**b**) operation: The grid voltages, input capacitor voltages and output dc output voltage are highlighted in **x.i**, the applied duty cycles of phase a in **x.ii**, and the grid currents and the phase a inductor current in **x.iii**.

In case of single-phase operation all the ac-side (stage I) half-bridges are connected in parallel (to ensure proper current sharing with $i_\mathrm{a} = \frac{1}{3} i_\mathrm{abc}$ individual current controllers can be employed in each phase module), and, therefore, also the same grid u_a and input capacitor voltage u_an is applied to all the bridge-legs. As can be observed in **Fig.3x.i**, the input capacitor voltages are the sum of the output voltage, $U_\mathrm{dc} = 400\,\mathrm{V}$, and the respective grid voltage, e.g., u_a, independently of the operation in single-phase and three-phase mode. The applied duty cycle profiles d_AI and d_AII according to equations (3) and (4), respectively, in **Fig. 3x.ii** result in a mutually exclusive high-frequency switching operation of the two bridge-legs A_I and A_II in phase module a with reduced switching losses as only three out of six half-bridges are switched simultaneously in the rectifier system. Last, the phase currents and the module inductor current of phase a shown in **Fig. 3 x.iii** highlight how the low-frequency inductor current stress (5) increases during mode I operation.

The simulation results prove the ability of the proposed converter to operate in both grid situations with the same voltage and current stress in the power devices (for the same output power), which is the main benefit of the concept and enables nominal power three-phase *and* single-phase operation without requiring component overdimensioning [16].

Experimental Verification: In order to experimentally prove the feasibility of the proposed three-/single-phase bidirectional converter, the existing prototype system from [17] has been reconfigured according to **Fig. 1**. The prototype operates at a switching frequency of $f_\mathrm{s} = 100\,\mathrm{kHz}$, features 1200 V SiC power semiconductors, and further details are provided in **Tab. 1**. Again, the European grid with $U_\mathrm{ac} = 230\,\mathrm{V_{RMS}}$ / $f_\mathrm{ac} = 50\,\mathrm{Hz}$, an

Table 1: Details of the employed prototype system from [17].

Designator	Details
$T_\mathrm{I}/T_\mathrm{I}'$, $T_\mathrm{II}/T_\mathrm{II}'$	1200 V / 25 mΩ SiC MOSFETs[1]
$f_\mathrm{s} = 100\,\mathrm{kHz}$	ePWM modules of the TI TMS320F28335
$L = 85\,\mu\mathrm{H}$	2 × TDK N97 EELP 43 Ferrite Core, 20 turns
$C_\mathrm{a} = 1.3\,\mu\mathrm{F}$	6 × 0.47 µF / 1 kV Syfer X7R[2]

[1] note that 600 V power semiconductors would be sufficient for the dc-stage
[2] referenced evenly to the positive p and negative n dc output rails

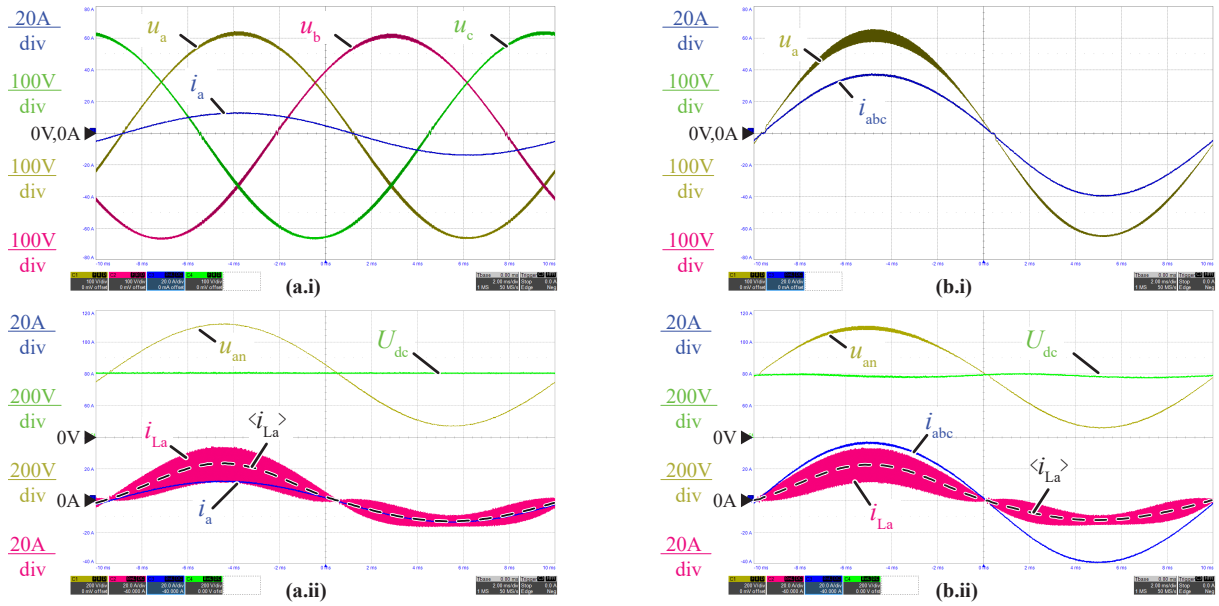

Fig. 4 *Experimental waveforms in open-loop modulation (i.e., inverter mode with a dc supply and a resistive load connected to the ac terminals a, b, c) with an output power of 6 kW in three-phase (**a**) and single-phase operation (**b**).*

x.i three-phase grid voltages $u_{\rm a}$,$u_{\rm b}$,$u_{\rm c}$ (or single-phase ac voltage $u_{\rm a}$) and phase a grid current $i_{\rm a}$ (or single-phase grid current $i_{\rm abc} = 3 \times i_{\rm a}$);
x.ii main converter waveforms of phase module a, i.e., input capacitor voltage $u_{\rm an}$, dc output voltage $U_{\rm dc}$, inductor current $i_{\rm La}$ and grid current $i_{\rm a}$.

output voltage $U_{\rm dc} = 400$ V, and a power level $P_{\rm abc} = 3 \times P_{\rm a} = 6$ kW is considered. Note that the system is operated in inverter mode, i.e., supplied from a dc source and with a resistive load connected to the ac terminals.

Fig. 4 presents the main experimental results of the proposed converter operating in both three-phase (**a**) and single-phase (**b**) configuration. In these figures, the grid voltages as well as the input grid current both in three-phase, u_a, u_b, u_c, and single-phase, $u_{\rm a}$, configuration can be seen to deliver the same output power. Experimental waveforms prove the ability of the proposed converter to achieve a smooth output voltage, $U_{\rm dc}$, regardless the operation mode. Moreover, the current through the phase a inductor, $i_{\rm La}$ remains the same regardless the grid situation. Thereby, the main advantage of the proposed converter, i.e., three-phase and single-phase operation under the same voltage and current stress of the main power components (thus enabling nominal power single-/three-phase operation without component overdimensioning) is verified.

Conclusion: Modern 400 V dc distribution systems for, e.g., industrial automation or robotics, are supplied by bidirectional PFC rectifiers which ideally can operate both from the three-phase and the single-phase grid. In this letter, a novel bidirectional universal single-/three-phase-input unity power factor differential ac-dc converter is presented. Unlike previous concepts, the proposed converter allows three-phase *and* single-phase operation with the same current and voltage stresses in the main power components regardless the available number of grid phases, hence representing a universal grid-input PFC rectifier. The proposed converter is analyzed theoretically and simulated. Experimental results using a 6 kW converter operating with a switching frequency of 100 kHz prove the ability of the converter to process full power both in three-phase and single-phase configuration under the same component stress, thereby verifying the main benefits of the new concept.

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