Received: Added at production | Revised: Added at production | Accepted: Added at production

DOI: xxx/xxxx

ARTICLE TYPE

A novel bridgeless flying capacitor multilevel rectifier†

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Summary

A novel transformerless three-phase unidirectional bridgeless flying capacitor (UBFC) rectifier for medium-voltage and high-voltage applications is presented by this paper. The rectifier consists of three single-phase rectifiers in wye connection, the DC outputs of the three single-phase rectifiers are connected in parallel to provide a high common DC-link bus which makes it convenient to connect with NPC or FC multilevel inverters. To avoid phase to phase current circulation, an additional inductor and diode are added to each single-phase rectifier. Compared with conventional bidirectional multilevel converters, only half IGBTs are employed with lower voltage stress, line-frequency transformers are no longer be required, which makes the proposed rectifier has a series of advantages such as reduced cost, simplified control complexity, increased reliability and improved overall efficiency. The basic operating principle of the proposed rectifier in continuous conduction mode is discussed, an improved carrier-based level-shifted PWM modulation method integrated with voltage balancing and the double closed-loop control strategy are proposed to achieve more voltage levels and keep the flying capacitors in balance. The feasibility of proposed rectifier is verified by the simulation as well as experimental results.

KEYWORDS:
Bridgeless multilevel rectifier, transformerless, capacitors voltage balancing control, high voltage DC-link bus

1 | INTRODUCTION

The multilevel converter has been widely used in the fields of high-voltage high-power adjustable speed motor drives, active power filter (APF), high voltage direct current transmission (HVDC) and reactive power compensation .[1] The most typical multilevel converters are neutral point clamped (NPC),[2,3] cascaded H-Bridge (CHB)[4] and flying capacitor (FC) .[5] In order to achieve the high voltage power transformation[6] by using low voltage power electronic devices, and mitigate input current harmonics, the bulky line-frequency (LF) phase-shifted transformers have always been used for isolation in such multilevel converters.

The LF trasformerless converter attracts attention in the field of power electronics technology for years. There are types of such system configurations: 1) the back-to-back (BTB) connection of a NPC PWM rectifier and inverter ,[7] 2) a front-end diode rectifier connected with NPC PWM inverter.[8,9] Considering in quite a lot industrial applications, bidirectional power flow is not required, [10,11] such as the AC adjustable speed motor drives with pumps or fans load, for such applications, the first configuration seems too complex and costly. In the latter a passive or an active filter is required in front end to mitigate input current harmonics

†A novel bridgeless flying capacitor multilevel rectifier.

[0]**Abbreviations:** ANA, anti-nuclear antibodies; APC, antigen-presenting cells; IRF, interferon regulatory factor

produced by the diode rectifier, besides, it requires additional hardware installation to achieve voltage balancing control [12,13] of the DC-link split capacitors. [14]

The cascaded multilevel converter based on high-frequency (HF) isolated DC/DC converter is another type of LF transformerless converter where the traditional LF transformers are removed. [15,16,17] Such multilevel converters have attracted more and more attentions in recent years due to their many advantages, such as high power factor on the grid side, low voltage stress of the device, flexibility of control and high power density. [18] However, up to now, such converters still cannot be widely used in high-voltage and high-power applications, the reason is that the high power high frequency isolated DC/DC converter with high efficiency and high power density is very difficult to design and to implement. [19]

Itoh J. et al. [20] proposed a unidirectional inverter uses half the number of switches in comparison to the NPC and FC types. Several multilevel unidirectional topologies have been proposed in the literature. [21,22,23] However, in distribution of losses among the devices is not equal, extra hardware circuitry is required to balance the DC-link capacitor voltages. Cheng H. et al. [24] proposed a unidirectional three-phase multilevel rectifier with transformerless (either LF or HF transformer isolation) system. The topology features fewer active switches with lower voltage stress to achieve high-voltage common DC-link bus. However, due to the rectifier stage of the converter is composed of three single-phase diode bridge rectifiers in star-connection, the three single-phase rectifiers provide three pairs of DC-link bus instead of one common DC-link bus, which limits it to connect directly with traditional three-phase NPC or FC multilevel inverters. Besides, bigger capacitor is required in the three pairs of DC-link bus to mitigate the bigger voltage ripples composed of mainly secondary order harmonics in each DC-link.

This paper proposes a novel transformerless three-phase unidirectional bridgeless flying capacitor (UBFC) rectifier. In which, the number of cascaded modules can be conveniently adjusted according to the required load voltage and supply voltage levels, and there is no need to use either the LF transformers or HF DC/DC modules for isolation. Compared with the typical full controlled clamped type of multilevel converters, such as NPC or FC converters, for the same output voltage levels, the proposed topology can greatly reduce the number of employed active power switches, as well as the voltage stress of each power device. As consequence, reduce the cost, simplify the control complexity, meanwhile, increase its reliability and improve the overall efficiency of the converter. Compared with the three-phase unidirectional multilevel converters proposed by Hong Cheng et al., [24] the proposed topology can be used in higher voltage level, can form one common DC-link bus instead of three pair of DC-link, so that it can be connected directly with the traditional NPC or FC multilevel inverters. Besides, the ripples composed of mainly six order harmonics is much lower that means only less capacitance is required. The comparisons of varies *m*-level rectifiers are list in Table 1 in Section 2.

The rest of this paper is organized as follows. Section 2 presents the working principles of the proposed rectifier, at first , the single-phase rectifier topology with *M* modules in cascading is described, then taking three-level rectifier as an example, the current flowing paths are analyzed and the steady state mathematical model is established. In Section 3, the parallel connection method of three pairs of DC output of three single-phase bridgeless rectifiers is discussed, including the applicable structure for restraining interphase circulating current, and the analysis of current sharing characteristics. On this basis, carrier-based PWM modulation and double closed-loop control strategy with flying capacitors voltage balancing control is presented in Section 4. Simulation and experimental results are provided in Section 5 to verify the validity of the proposed topology, the control strategy and the parameter design method. Conclusion is drawn in Section 6.

2 | CIRCUIT DESCRIPTION

2.1 | Configuration of the UBFC Rectifier Topology

The single–phase UBFC multilevel rectifier is shown in Figure 1. The rectifier is a boost circuit. A common DC-link bus can be formed on the DC side.

This paper takes the example of a three-level rectifier topology as shown in Figure 2. S_i and D_i (i=1, 2, 3, 4) are active switches and fast recovery diodes, respectively. u_i,u_{ab}, u_o are the grid voltage, the input voltage of the rectifier, and the DC-link voltage. u_{C1} and u_{C2} stand for the flying capacitor (C_1 and C_2) voltages respectively. i_L is the current flowing through the boost inductor L that equals to the power supply current. R is the equivalent resistance of the load.

The rectifier has two bridge arms that each bridge can generates three voltage levels, and the voltage uab between two arms is five levels. m is the number of voltage level. Based on the research of three-level rectifier topology, an arbitrary m-level rectifier analysis can be deduced from that, like operating states circuit under continuous conductivity, expressions of the converter under steady-state, and key parameters of topology.

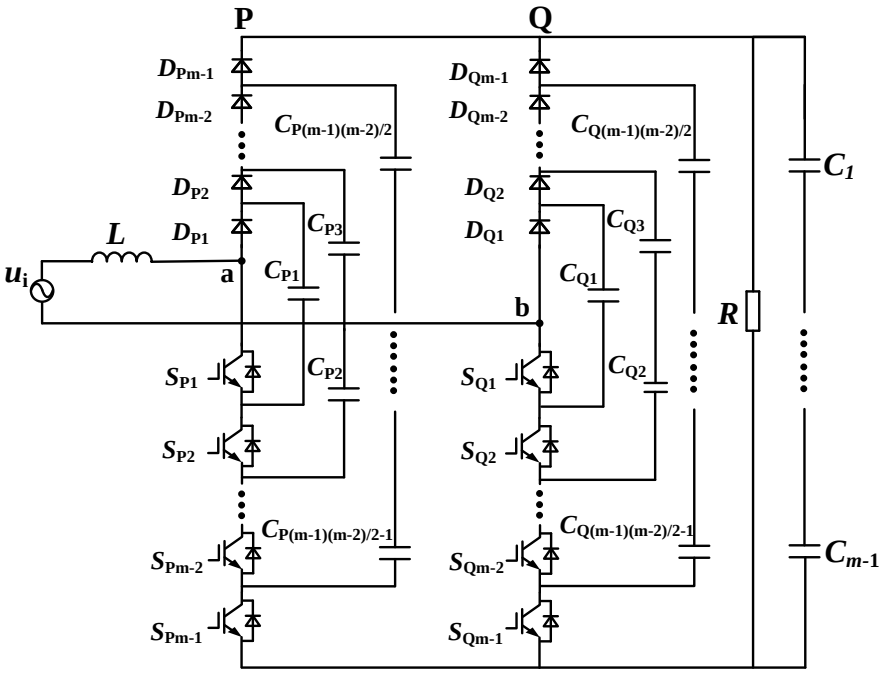

Figure 1 Proposed UBFC multilevel rectifier with a common DC-link bus.

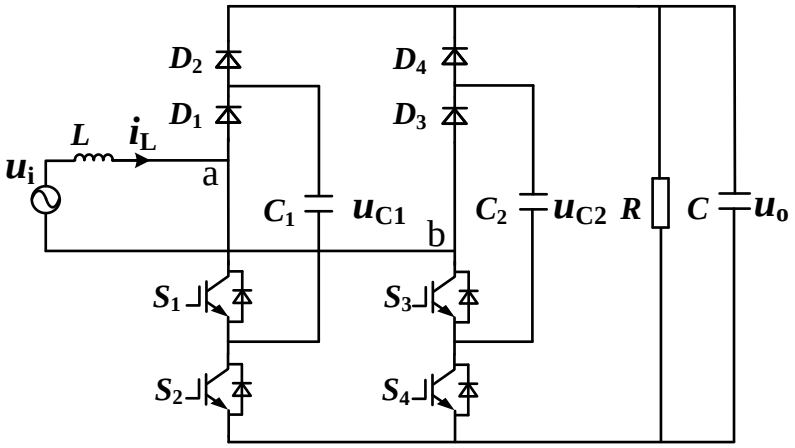

Figure 2 The single-phase three-level UBFC rectifier topology.

There are some assumptions that the switching frequency of switching device is much higher than that of the power supply voltage, the capacitors C , C_1 and C_2 are large enough to make the voltage of u_o, u_{C1} and u_{C2} approximately remain constant, the switches S_i and fast recovery diodes D_i are ideal.

The comparison of different single-phase topologies listed in Table 1. It can be seen from the table that the number of switches in UBFC converter is half of the NPC, CHB and FC. NPC and CHB topologies have no flying capacitors, but when the number of the output voltage level increases, the control strategy will be complex. Since the UBFC converter has fewer switches, the control complexity is simplified. Compared with cites[21] and[22], less HF diodes have been used.

There are totally 8 operating states when the system is working on continuous conduction mode (CCM) and steady state, as shown in Figure 3. When the rectifier works in the positive half period of the input current, the operating states are only

Table 1 Comparison of different single-phase topologies.

Converter	Switches	Flying capacitors	HF Diode	Control complexity
Bidirectional				
NPC	$2(M-1)$	0	$M-1$	medium
CHB	$2(M-1)$	0	0	high
FC	$2(M-1)$	$(M-1)(M-2)/2$	0	medium
Unidirectional				
[21]	$(M-1)$	0	$3(M-1)$	medium
[22]	$2(M-1)$	0	$2(M-1)$	high
UBFC	$(M-1)$	$(M-1)(M-2)/2$	$M-1$	low

Table 2 The changes of each operating state under different modes.

States	S_1	S_2	S_3	S_4	L	C	C_1	C_2	u_{ab}	Voltage Levels
1	0	0	X	X	D	C	C	N	u_o	u_o
2	0	1	X	X	D	D	C	N	u_{C1}	u_o /2
3	1	0	X	X	D	C	D	N	u_o -u_{C1}	-u_o /2
4	1	1	X	X	C	D	N	N	0	0
5	X	X	0	0	D	C	N	C	u_o	u_o
6	X	X	0	1	D	D	N	C	u_{C1}	u_o /2
7	X	X	1	0	D	C	N	D	u_o -u_{C2}	-u_o /2
8	X	X	1	1	C	D	N	N	0	0

"C" stands for "charging", "D" stands for "discharging", "N" stands for "constant".

determined by S_1 , S_2. Similarly, in the negative half period, the states are only determined by S_3, S_4. It shows that all the switches have the same conduction time in one switching period. We classify all the states into two categories: one is the AC current operating in the positive half period, and the other is operating in the negative half period. Each active switch can operate in two states, "on" corresponds to "1" state and "off" corresponds to "0" state. that is:

$$S_i = \begin{cases} 1 & \text{on}, \\ 0 & \text{off}. \end{cases} \tag{1}$$

According to the above eight switching modes, the charging/discharging changes of components on each operating state are shown in Table 2. The voltage stress of S_1 and S_2 are given by

$$u_{S1,S2} = u_o - u_{C1}, \tag{2}$$

$$u_{S3,S4} = u_o - u_{C2}. \tag{3}$$

In order to maintain the equal voltage stress of each switch, the following equation should be satisfied:

$$u_{S1,S2} = u_{S3,S4} = u_{C1} = u_{C2} = \frac{u_o}{2}. \tag{4}$$

2.2 | Steady-state Circuit Analysis and Equation of States

When the converter operates on the positive half period of the input current, two switches S_1 and S_2 have four operating states (S_1, S_2), namely (0, 0), (0, 1), (1, 0), (1, 1), the equivalent circuit of four operating states shown in Figure 4. When the circuit is in the state (0, 0), applying KVL and KCL to the topology shown in Figure 4(1), the steady-state mathematical model can be

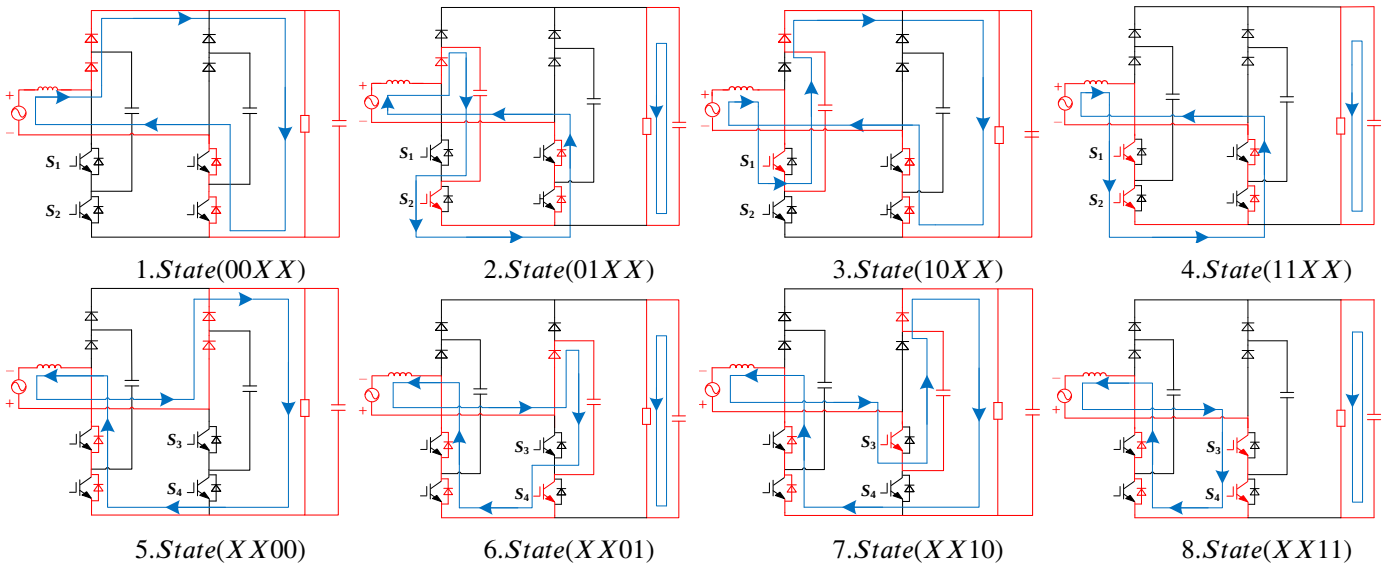

Figure 3 The 8 operating states in continuous conduction mode.

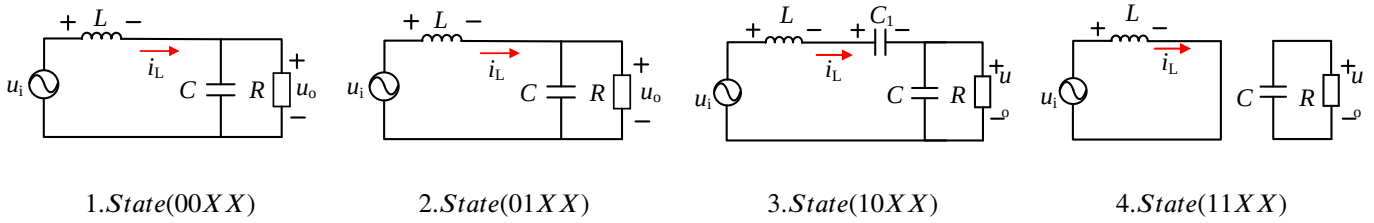

Figure 4 The equivalent circuit of the positive half period of the input current.

yielded as:

$$\begin{cases} \frac{di_L}{dt} = u_i - u_o, \\ \frac{du_o}{dt} = i_L - i_R = i_L - \frac{u_o}{R}. \end{cases} \tag{5}$$

After simplification, (5) can be rewritten as:

$$\begin{cases} \frac{di_L}{dt} = -\frac{1}{L}u_o + \frac{1}{L}u_i, \\ \frac{du_o}{dt} = \frac{1}{C}i_L - \frac{1}{RC}u_o. \end{cases} \tag{6}$$

Selecting the inductive current i_{L} and capacitors voltage u_{o}, u_{C1} and u_{C2} as state variables, when State 1:$(S_1, S_2) = (0,0)$, the equations can be obtained as:

$$\begin{pmatrix} \frac{di_L}{dt} \\ \frac{du_o}{dt} \\ \frac{du_{C1}}{dt} \\ \frac{du_{C2}}{dt} \end{pmatrix} = \begin{pmatrix} 0 & -\frac{1}{L} & 0 & 0 \\ \frac{1}{C} & -\frac{1}{RC} & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{pmatrix} \begin{pmatrix} i_L \\ u_o \\ u_{C1} \\ u_{C2} \end{pmatrix} + \begin{pmatrix} \frac{1}{L} \\ 0 \\ 0 \\ 0 \end{pmatrix} u_i. \tag{7}$$

The analysis of other states is similar to the above, which will not be derived here, the state equation immediately given as follow:

State 2: $(S_1, S_2) = (0,1)$

$$\begin{pmatrix} \frac{di_L}{dt} \\ \frac{du_o}{dt} \\ \frac{du_{C1}}{dt} \\ \frac{du_{C2}}{dt} \end{pmatrix} = \begin{pmatrix} 0 & 0 & -\frac{1}{L} & 0 \\ 0 & -\frac{1}{RC} & 0 & 0 \\ -\frac{1}{C_1} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{pmatrix} \begin{pmatrix} i_L \\ u_o \\ u_{C1} \\ u_{C2} \end{pmatrix} + \begin{pmatrix} \frac{1}{L} \\ 0 \\ 0 \\ 0 \end{pmatrix} u_i. \tag{8}$$

State 3: $(S_1, S_2) = (1,0)$

$$\begin{pmatrix} \frac{di_L}{dt} \\ \frac{du_o}{dt} \\ \frac{du_{C1}}{dt} \\ \frac{du_{C2}}{dt} \end{pmatrix} = \begin{pmatrix} 0 & -\frac{1}{L} & \frac{1}{L} & 0 \\ \frac{1}{C} & -\frac{1}{RC} & 0 & 0 \\ -\frac{1}{C_1} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{pmatrix} \begin{pmatrix} i_L \\ u_o \\ u_{C1} \\ u_{C2} \end{pmatrix} + \begin{pmatrix} \frac{1}{L} \\ 0 \\ 0 \\ 0 \end{pmatrix} u_i. \tag{9}$$

State 4: $(S_1, S_2) = (1,1)$

$$\begin{pmatrix} \frac{di_L}{dt} \\ \frac{du_o}{dt} \\ \frac{du_{C1}}{dt} \\ \frac{du_{C2}}{dt} \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 & 0 \\ 0 & -\frac{1}{RC} & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{pmatrix} \begin{pmatrix} i_L \\ u_o \\ u_{C1} \\ u_{C2} \end{pmatrix} + \begin{pmatrix} \frac{1}{L} \\ 0 \\ 0 \\ 0 \end{pmatrix} u_i. \tag{10}$$

The equation of complete power period of the circuit is expressed as:

$$\dot{X} = AX + Bu. \tag{11}$$

The variable k is used to denote the positive or negative period: when k=1 means the rectifier is working on the positive period of the input power current, when k=0 means on the negative period.

The relevant simulation parameters of rectifier are given by:

$$\dot{X} = \begin{pmatrix} \frac{di_L}{dt} \\ \frac{du_o}{dt} \\ \frac{du_{C1}}{dt} \\ \frac{du_{C2}}{dt} \end{pmatrix}, X = \begin{pmatrix} i_L \\ u_o \\ u_{C1} \\ u_{C2} \end{pmatrix}, B = \begin{pmatrix} \frac{1}{L} \\ 0 \\ 0 \\ 0 \end{pmatrix}, u = u_i, \tag{12}$$

$$\mathrm{A}=\begin{pmatrix} 0 & -\frac{1}{L}\left[k\left(1-S_2\right)+(1-k)\left(1-S_4\right)\right] & \frac{1}{L}\left[k\left(S_1-S_2\right)\right] & \frac{1}{L}(1-k)\left(S_3-S_4\right) \\ \frac{1}{C}\left[k\left(1-S_2\right)+(1-k)\left(1-S_4\right)\right] & -\frac{1}{RC} & 0 & 0 \\ -\frac{k}{C_1}\left(S_1-S_2\right) & 0 & 0 & 0 \\ -\frac{1-k}{C_2}\left(S_3-S_4\right) & 0 & 0 & 0 \end{pmatrix}, \tag{13}$$

$$\begin{cases} \frac{di_L}{dt} = -\frac{1}{L}\left[k\left(1-S_2\right)+(1-k)\left(1-S_4\right)\right]u_o + \frac{1}{L}\left[k\left(S_1-S_2\right)\right]u_{C1} + \frac{1}{L}\left[(1-k)\left(S_3-S_4\right)\right]u_{C2} + \frac{1}{L}u_i, \\ \frac{du_o}{dt} = \frac{1}{C}\left[k\left(1-S_2\right)+(1-k)\left(1-S_4\right)\right]i_L - \frac{1}{RC}u_o, \\ \frac{du_{C1}}{dt} = -\frac{k}{C_1}\left(S_1-S_2\right)i_L, \\ \frac{du_{C2}}{dt} = -\frac{1-k}{C_2}\left(S_3-S_4\right)i_L. \end{cases} \tag{14}$$

It is assumed that the switching period is T_s, by using the moving average model, the switching period average of S_i described in (1) are given by

$$S_i(t)_{T_S} = \frac{1}{T_S}\int S_i(t)\,dt = d_i(t), \tag{15}$$

where d_i is the duty cycle of switches S_i, $i = 1, 2, 3, 4$. When the system is in steady-state, the duty factor d_i are given by

$$d_1 = d_2 = d_3 = d_4 = d. \tag{16}$$

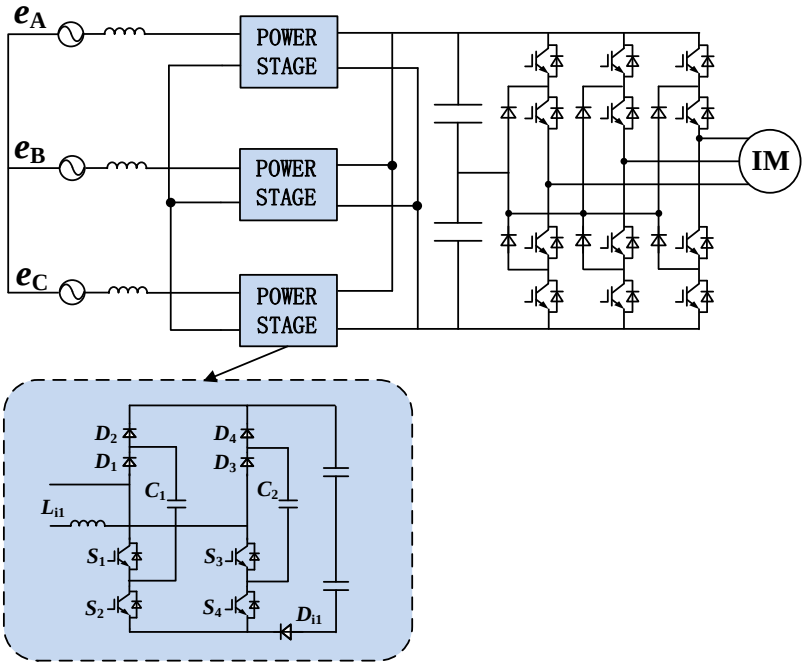

Figure 5 The proposed three-phase UBFC rectifier in wye connection connected to NPC inverter.

Applying the volt-second balance and ampere-second balance principles to (14) yields:

$$\begin{cases} u_i = (1-d)\,u_o, \\ i_L = \frac{u_o}{(1-d)R}. \end{cases} \tag{17}$$

The relationship of the rectifier can be obtained as:

$$\frac{u_o}{u_i} = \frac{1}{1-d}. \tag{18}$$

Thus, the duty factor d can be yielded as:

$$d = 1 - \frac{u_i}{u_o}. \tag{19}$$

On steady-state, u_{i} is constant while u_{i} changes sinusoidally with time, as a result shown in equation (19) that d also changes sinusoidally with time.

Assuming that V_{m} is the amplitude of u_{i}, d minimizes when u_{i} is equal to V_{m}. Similarly, d maximized when u_{i} is equal to zero. It can be concluded that the range of values of d is:

$$1 - \frac{V_m}{u_o} \leq d \leq 1. \tag{20}$$

3 | THE CONFIGURATION OF THREE-PHASE TOPOLOGY

3.1 | The Three-phase UBFC Converter

The main advantage of this novel rectifier is that when it connected to a NPC inverter in medium-voltage application, there is no need to use transformer for isolation. The three-phase UBFC rectifier converter topology is shown in Figure 5.

The circuit of each phase is different from the single-phase topology that every stage has an independent input inductor L_{j1} and an independent continuous current diode D_{j1} ($j = 1, 2, 3$). These components are added to avoid phase to phase circulation.

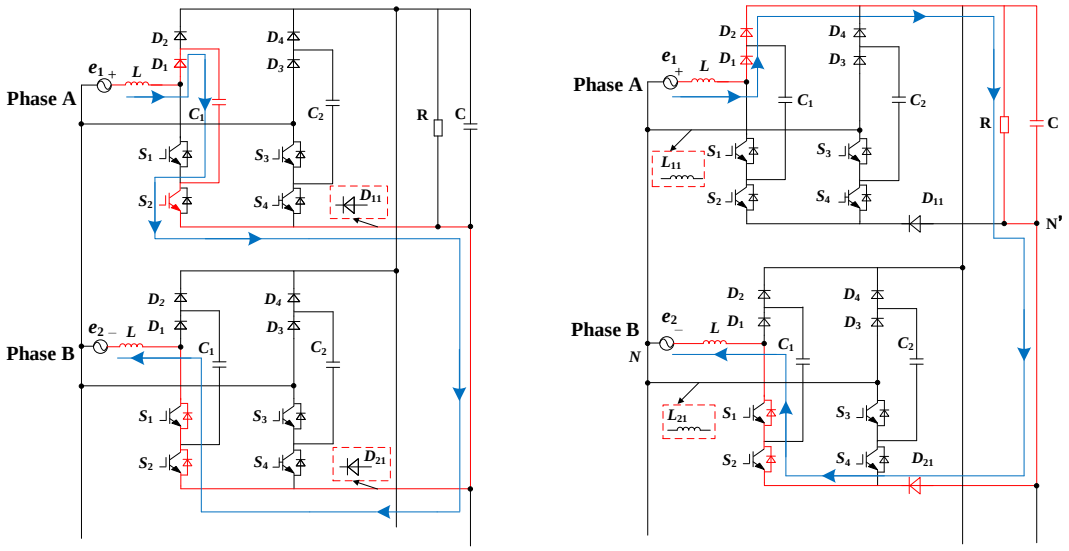

Figure 6 Phase to phase current circulation when e_1>0 and e_2<0. (a) add freewheeling diodes. (b) add inductors in the AC side.

3.2 | The Restraining of the Phase to Phase Current Circulation

In order to make the wye connection of the circuit work normally, it's necessary to understand that every single-phase circuit is operating independently, that is arbitrary switching state of all the switches are possible. Therefore, when several switches are on or off simultaneously, the current in one module can return from another module, which is inevitable.

Take any two modules as an example shown in Figure 6. In the case of an opposite signal in the input phase voltage, that is e_1>0 and e_2<0, under the circumstance (S_1=0 and S_2=1) or (S_1=S_2=1) in phase A, shown in Figure 3(2) (4), the current from the phase B will flow throw the inverse diodes which parallel with S_1 and S_2 of phase B, leads to the phase to phase circulation. To avoid this, in every phase a freewheeling diode D_{j1} has been added shown in Figure 6(a). The existence of a diode prevents current from flowing from the negative end of one stage to another.

When (S_3=S_4=0) or (S_3=1 and S_4=0) in phase B, shown in Figure 3(5) (7), the point N' is at a negative potential with respect to the neutral point N, meanwhile (S_1=S_2=0) or (S_1=1 and S_2=0) in phase A, shown in Figure 3(1) (3), the current from the phase A will first pass the load and then go throw the inverse diodes which parallel with S_1 and S_2 of phase B, also leads to the phase to phase circulation. By inserting an inductor L_{i1} in the AC side in Figure 6(b) keeps the point N' at a positive potential with respect to the neutral point N, which makes the current flow to the negative point among one phase.

4 | CONTROL AND MODULATION MODULATION STRATEGY

The main control goals that should be satisfied are as follows: obtain multilevel voltage, maintain the common DC-link voltage constant, remain the flying capacitor balanced and achieve unity input power factor. To achieve these goals, a combination of control and modulation strategy is adopted in the paper. To obtain multilevel voltage, carrier-based level-shifted PWM modulation method has been used for modulation. Double closed-Loop control strategy is adopted to enable the rectifier operate at a given DC-link voltage and maintain constant. Since the flying capacitors are in charging/ discharging stages during different periods, the flying capacitors voltages will be unbalanced. Therefore, the capacitor voltage balancing control is necessary. So the control and modulation strategy includes three aspects above. The control block diagram of the system is presented in Figure 7.

4.1 | Multilevel Modulation Method

In order to generate five levels of voltage between two arms, a certain modulation strategy is needed. This paper adopts a carrier-based level-shifted PWM modulation method as shown in Figure 8. The values of the two carriers are [0, 1], [1, 2]. In the

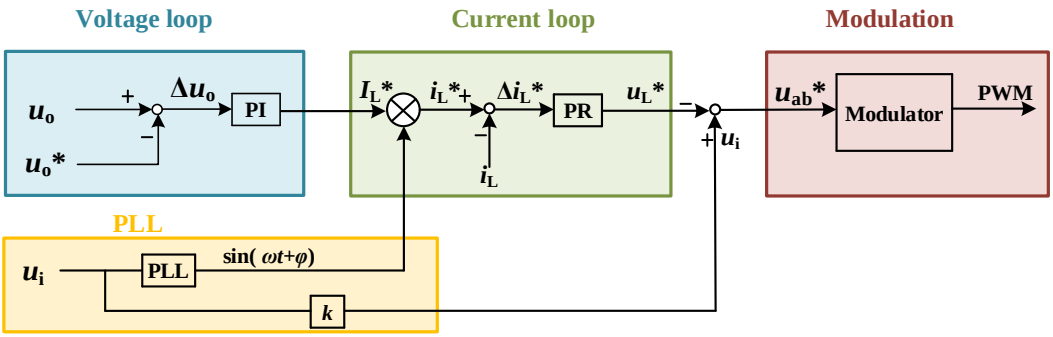

Figure 7 Control block diagram of the system.

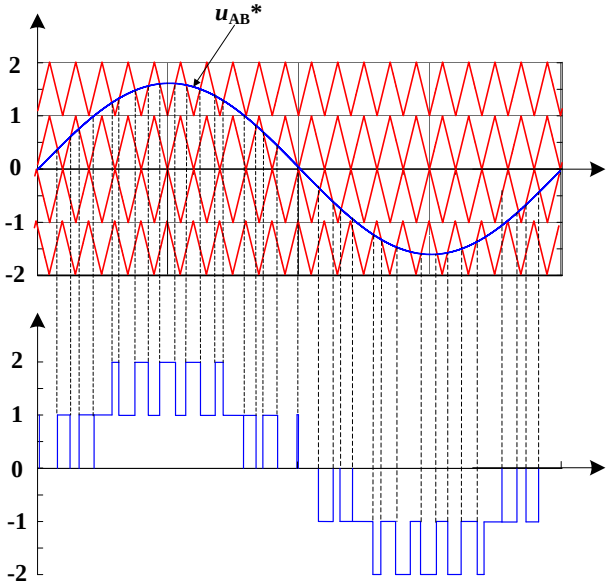

Figure 8 Carrier-Based Level-Shifted PWM modulation Method.

positive half period, two carriers are compared with the modulation wave u_{ab}*, the results are divided into two intervals: [0, 1], [1, 2]. When u_{ab}* is in the range of [0, 1], it is compared with the carrier wave with the range of [0, 1]. When u_{ab}* falls within the range [1, 2], it is compared with the carrier wave with the range of [1, 2]. As can be seen from the Figure 8, within half a cycle, three levels output voltage can be obtained through the on and off states of two switches. Therefore, in one cycle, S_1, S_2, S_3 and S_4 work in positive and negative cycle respectively to obtain five-level output voltage.

4.2 | The Double Closed-loop Control Strategy

The output signal of the voltage loop is taken as the input current reference of the current inner loop. With help of the phase-locked loop, the reference current signal output by the outer loop voltage controller can be expressed as:

$$i_i^* = [k_{pv}(u_o^* - u_o) + k_{iv}\int (u_o^* - u_o)dt]\frac{u_s}{V_m}\sin(\omega t + \varphi), \tag{21}$$

where k_{pv} is proportional gain, k_{iv} denotes the integrational gain. V_m and φ are the amplitude and phase information of the power supply voltage, respectively.

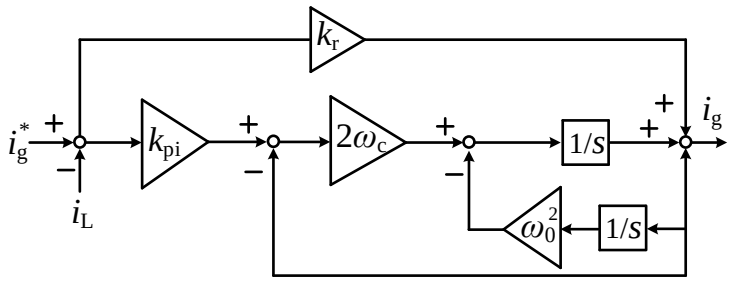

Figure 9 Block diagram of the current loop transfer function.

The current loop is used to control the input current by taking advantage of the proportional-resonance (PR) control to accurately track the AC reference current signal and ensure that it is in phase with the mains voltage. As a consequence, this proposed topology features fewer active switches can achieve high input power factor. The transfer function of PR controller is as follows:

$$G_i = k_{pi} + \frac{2k_r w_c s}{s^2 + 2k_r w_c s + {w_0}^2}, \tag{22}$$

where k_{pi} and k_{r} are proportional gain and resonant gain respectively, ω_0 and ω_c represent the resonant frequency and cut-off frequency. Block diagram of the current loop transfer function is shown in Figure 9.

4.3 | Control Strategy to Balance the Flying Capacitors

The above analysis is based on the flying capacitor voltage balance state. It suggests that the capacitor voltage balancing plays an important role in ensuring the normal operation of the rectifier. Although the multilevel converters have automatic voltage equalization characteristics, it takes a long time to adjust the capacitor voltage when the input voltage and load current change suddenly. In the actual circuit, due to the inconsistency of various switching characteristics and the asymmetry of each drive circuit, the capacitor voltage will deviate from the given voltage. Therefore, it is necessary to effectively control the capacitor voltages balancing in the multilevel converter. In steady stage, equation (14) equals to zero. The relationship between output voltage and flying capacitors can be expressed as:

$$u_o = \frac{\left[k\left(d_1 - d_2\right)\right] u_{C1} + \left[(1-k)\left(d_3 - d_4\right)\right] u_{C2}}{k\left(1 - d_2\right) + (1-k)\left(1 - d_4\right)}. \tag{23}$$

The voltage variation Δu_{C1} and Δu_{C2}can be expressed as:

$$\begin{cases} \Delta u_{C1} = -\frac{k}{C_1}\left(d_1 - d_2\right) i_L T_s, \\ \Delta u_{C2} = -\frac{1-k}{C_2}\left(d_3 - d_4\right) i_L T_s. \end{cases} \tag{24}$$

Equation (24) shows that the flying capacitor voltage variation Δu_{C1} and Δu_{C2} are dependent upon the duty cycle d_{i} of connected active switches.

Since C_1 and C_2 are in charging and discharging states in different period during one T_{s} that caused the unbalance duty cycle Δd_i. Assuming that the capacitors are large enough to keep the voltages u_{C}, u_{C1} and u_{C2} approximately constant and u_{o}=2u_{C1}= 2u_{C2}, d_{a} is the duty cycle at this point. Thus, under the unbalanced loads the duty cycle of each switch can be expressed as:

$$\begin{cases} d_1 = d_a + \Delta d_1, \\ d_2 = d_a + \Delta d_2, \\ d_3 = d_a + \Delta d_3, \\ d_4 = d_a + \Delta d_4, \end{cases} \tag{25}$$

where the Δd_i is the duty cycle difference, which is employed to compensate the loads difference.

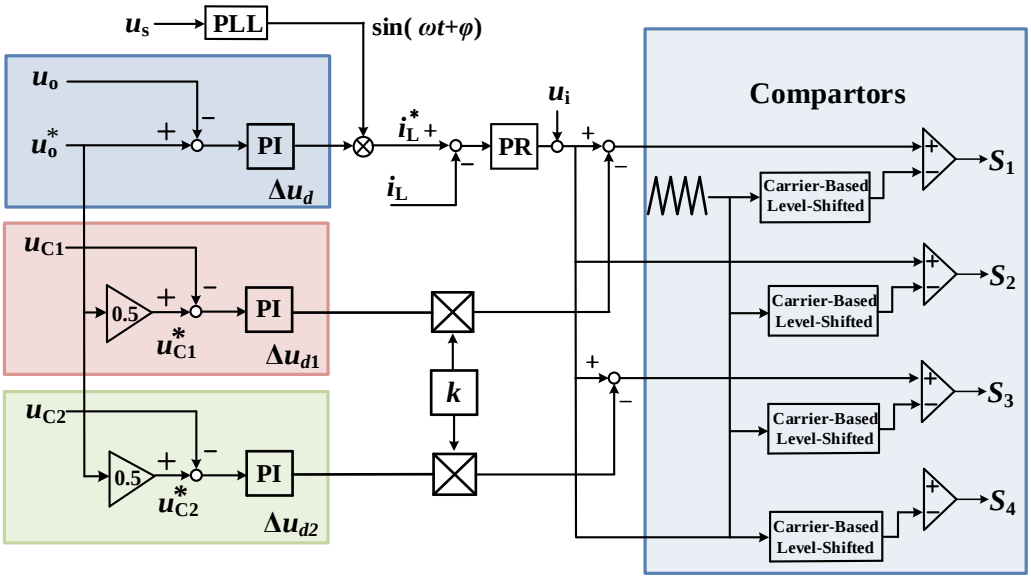

Figure 10 The overall control strategy diagram of the rectifier.

In steady stage, du_o/dt=0. Substituting (25) into (14), it can be obtained as:

$$u_C = R\left[k\left(1-d_a\right)+(1-k)\left(1-d_a\right)-k\Delta d_2-(1-k)\,\Delta d_4\right] i_L. \tag{26}$$

From (26) it can be deduced that DC-link voltage is affected by S_2 and S_4 on-off state. In order to avoid affecting the DC-link voltage and keep it constant at the reference, based on (26) the following equation should be satisfied:

$$\begin{cases} -k\Delta d_2-(1-k)\,\Delta d_4=-\Delta d_2=0 & k=1, \\ -k\Delta d_2-(1-k)\,\Delta d_4=-\Delta d_4=0 & k=0. \end{cases} \tag{27}$$

Substituting (25) and (27) into (24), it can be obtained the voltage variation:

$$\begin{cases} \Delta u_{C1}=-\frac{k}{C_1}\left(d_1-d_2\right) i_L T_s=-\frac{k}{C_1}\Delta d_1 i_L T_s, \\ \Delta u_{C2}=-\frac{1-k}{C_2}\left(d_3-d_4\right) i_L T_s=-\frac{1-k}{C_2}\Delta d_3 i_L T_s. \end{cases} \tag{28}$$

Figure 10 shows the block diagram of the overall control strategy of the rectifier.

5 | SIMULATION AND EXPERIMENTAL VERIFICATION

To better illustrate the principle of the proposed topology and the control method, a simulation case are carried out in MATLAB/Simulink and experimental results of a downscaled prototype are presented. The parameters employed by simulation model and experiment prototype are listed in Table 3.

The simulation takes the example of 1140V voltage level in the AC side. The waveforms of the novel topology are shown in Figure 11 to 15. The power supply voltage u_i and input current i_L are illustrated in Figure 11 which demonstrates the validity of unity power factor. Figure 12 depicts the harmonics spectrum of the input current, the THD is 2.44% which satisfied the demand of current quality. It's seen from Figure 13 that the AC input voltage achieved five levels in single-phase rectifier which is consistent as expected. In order to examine the dynamic response of the rectifier, the disturbance is added to the circuit simulation as shown in Figure 14 and 15. Figure 14 gives the waveforms of the inductor current i_L and DC-link voltage u_o when the load resistance R jumps from 37.5 Ω to 75 Ω at the point of 1s, it's obvious that the system can maintain balance even with sudden changes in load. Figure 15 shows the flying capacitors waveform under voltage balancing control with load sudden change.

In addition to the simulation, a downscaled prototype was been built to validate the performance of the configuration shown in Figure 16. The AC voltage amplitude is 110V and DC-link voltage reference is 200V. The main modulation and control

Table 3 Ratings an circuit parameters.

Parameters	Experimental	Value
Power rating P	90kW	388W
AC voltage vm	1140V	110V
DC-link voltage vo	2400V	200V
Switching frequency fs	10kHZ	10kHZ
Input Filter inductor L	5mH	3mH
Output capacitor C	2000uF	1000uF
Flying capacitor C1, C2	100uF	100uF

algorithms are implemented in TMS320F28335. The experimental waveforms are shown in Figure 17 to 19. Similar to the simulation, Figure 17 display the waveforms of power supply voltage u_{i} and input current i_{L}, proving that the rectifier can operate under unity power factor. Figure 18 shows the three voltage levels of each arm. Figure 19 shows the DC-link voltage u_{o} and input current i_{L} experimental waveforms under imbalanced loads, when the load resistance R jumps from 100 Ω to 200 Ω, the system can maintain balance even with sudden changes in load by the balancing control strategy.

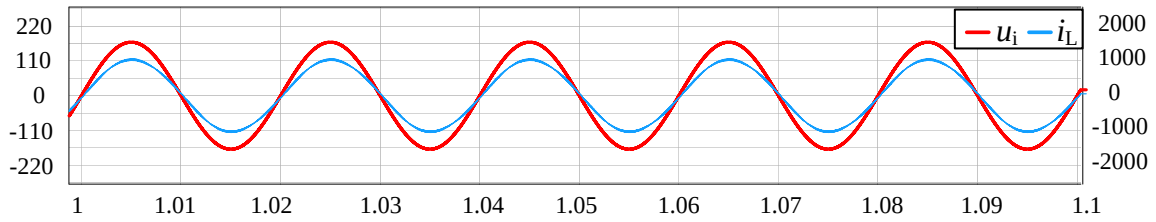

Figure 11 The power supply voltage u_{i} and input current i_{L} simulation waveforms.

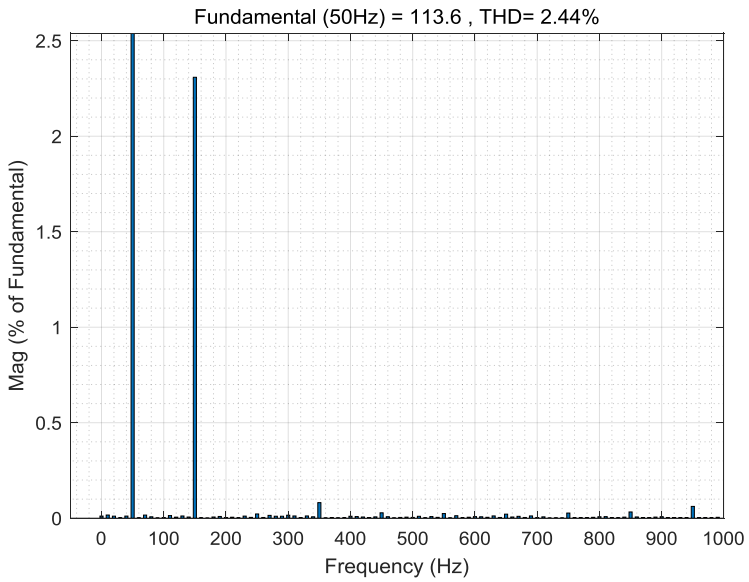

Figure 12 THD analysis of input current i_{L}.

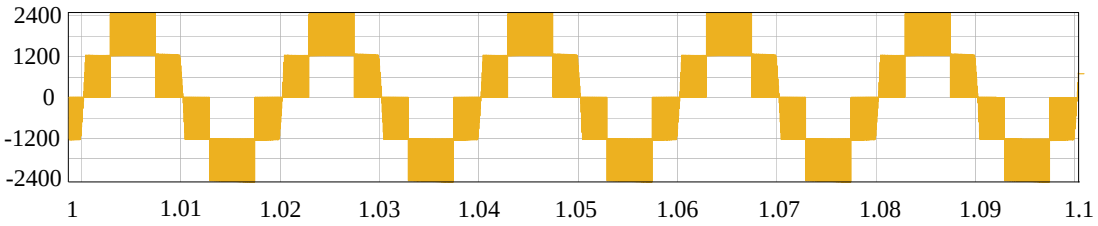

Figure 13 The simulation waveform of input voltage of the diode rectifier.

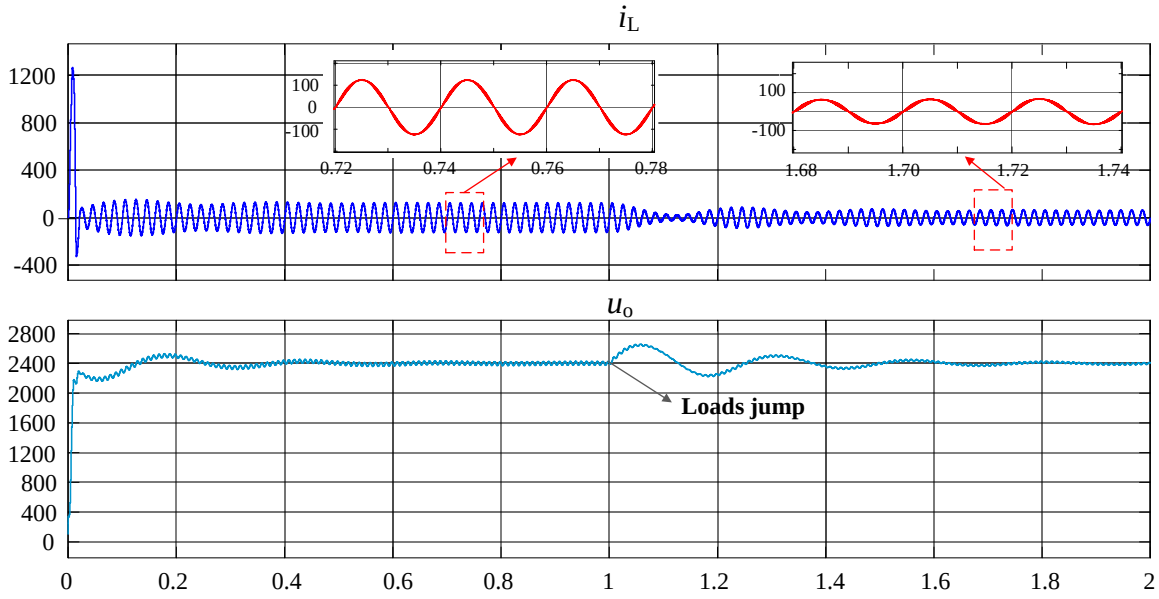

Figure 14 The inductive current i_L and dc-link voltage u_o simulation waveforms under the imbalanced loads.

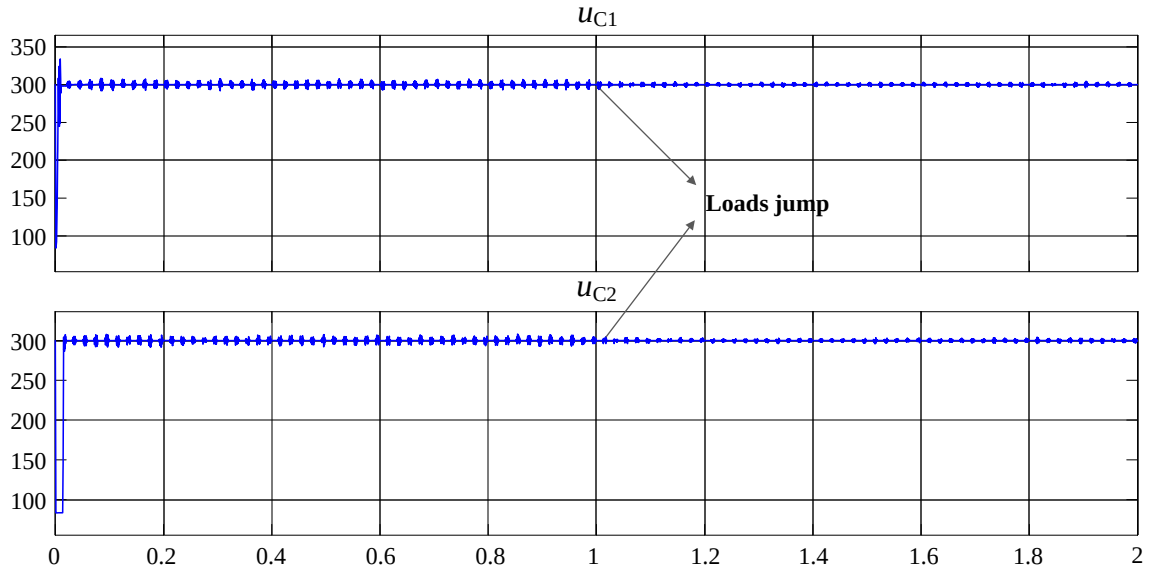

Figure 15 The flying capacitor voltage u_{C1} and u_{C2} simulation waveforms.

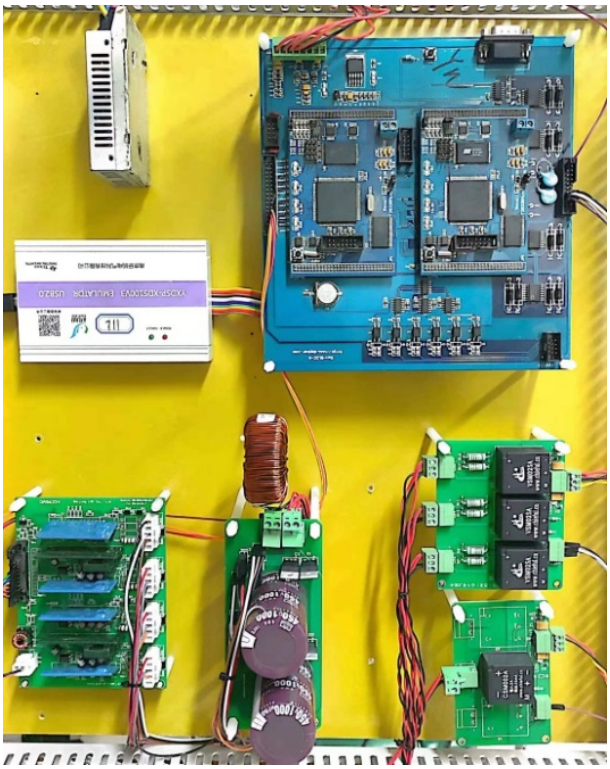

Figure 16 The downscaled experiment prototype.

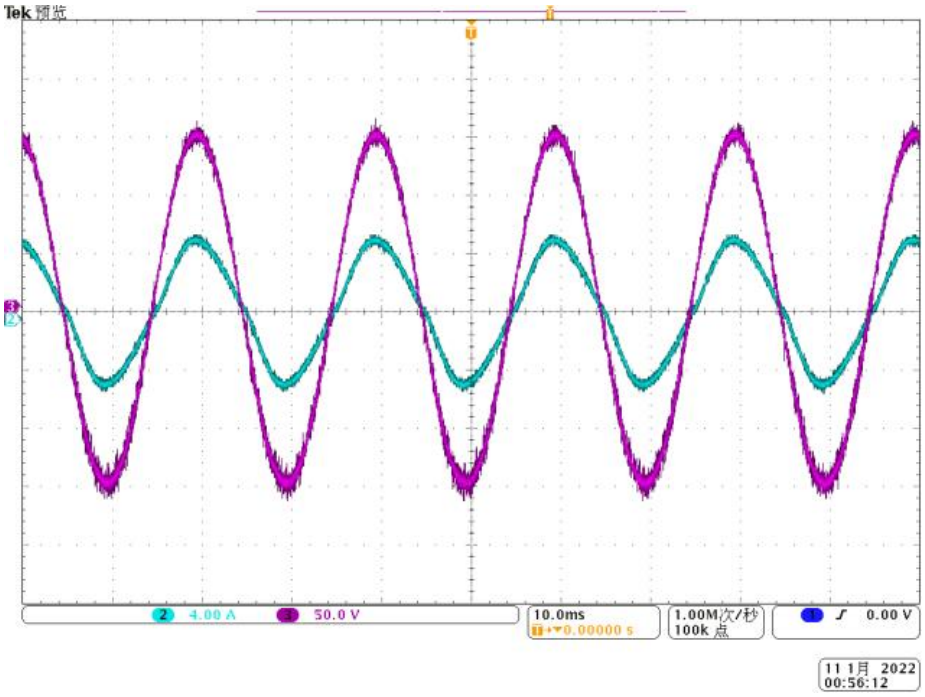

Figure 17 The power supply voltage $v_s$vs and input acurrent i_L experimental waveforms.

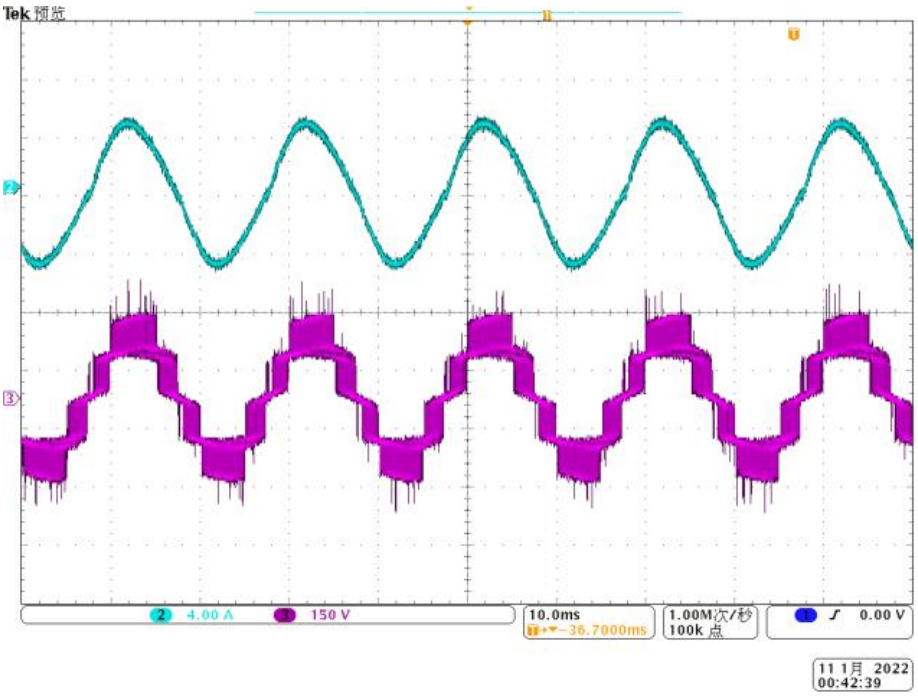

Figure 18 The three voltage levels experimental waveforms.

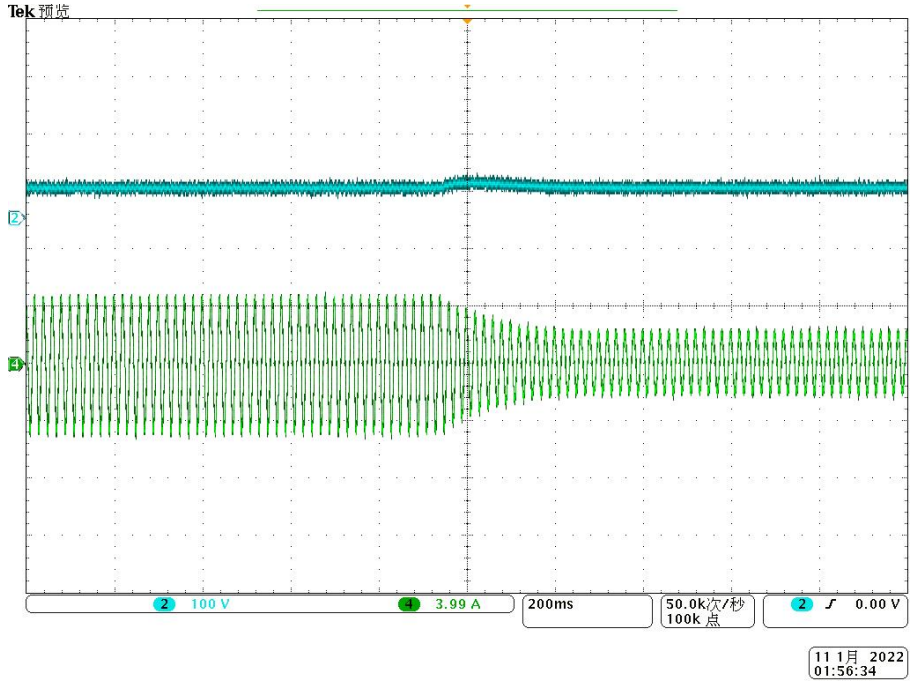

Figure 19 The dc-link voltage u_o and input current i_L experimental waveforms under imbalanced loads.

6 | CONCLUSION

A novel bridgeless flying capacitor multilevel rectifier for medium or high voltage transformerless conversion applications is proposed in the paper. The converter provides a variety of main power circuits, each of which is composed of expandable module units for forming common DC-link. It overcomes the disadvantage of unable generating high DC-link voltage due to the voltage stress limitation of the power switch. Different topology configurations can be selected according to the needs of different voltage levels. Since half of active switches have been replaced by fast recovery diodes leads to less drivers, lower cost and reduced control complexity. Another main advantage of this novel rectifier is that when it connected to an inverter in high-frequency or high-voltage application, there is no need to use transformer for isolation. In many power converters, line-frequency transformers account for a large part of the cost. It is of great significance to design a converter without line-frequency transformers which can be used in high power conversion.

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How to cite this article: Y.P Li, H. Cheng, C. Wang, Z.H. Zhao W. Yuan, and J. Wang (2023), A novel bridgeless flying capacitor multilevel rectifier, *Q.J.R. Meteorol. Soc.*, *2017;00:1–6*.