A power cycling circuit for switched-capacitor arrays

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Switched capacitor array (SCA) circuits allow a fast acquisition of short signals as samples in memory cells, being an alternative to conventional converter circuits. Each memory cell of an SCA has a readout buffer circuit needed only during a short time, thus wasting power when is left ON. Presented is the design of a power cycling circuit that greatly reduces power consumption of SCA circuits by turning buffers ON only when needed. Results from circuit simulations of a prototype implementation are presented. The reduction on power consumption of SCA circuits with power cycling are computed from the results and compared to conventional circuits.

Introduction: Switched-capacitor array (SCA) circuits have seen their application as an analog memory for fast signal acquisition [1–4]. The basic structure of an SCA, shown in Fig. 1, consists of an array of memory cells that store voltage samples in capacitors, either as single ended or differential value. Samples are written to the cells in a sequential fashion via switches that connect the capacitor of each memory cell to the circuit input, and are readout also in a sequential fashion, by connecting one memory cell at a time to the output, usually via the action of an external clock that cycles a one-hot readout shift register.

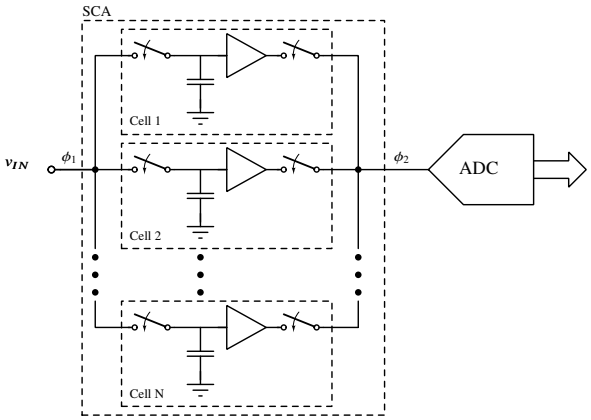

Fig 1 *SCA circuit block diagram.*

As the voltage sample in a memory cell is held as a charge in a capacitor, a buffer is necessary between its plate and the output. Since a cell buffer circuit would only operate during the time a cell is being read, the rest of the time it is just wasting power. The more memory cells present in an SCA, the more power is wasted and thus the lower the efficiency of the circuit.

Design: A power cycling circuit is designed in this work that would greatly contribute to the efficiency of the SCA by shutting down the unused memory cell buffers, and only turning them on for the brief moment that they are operating during a cell read. A simplified block diagram is shown in Fig. 2. An OR gate with its inputs connected both to a previous and a next readout register, drives a toggle flip-flop that generates an enable signal for the buffers.

The enable signal for the nth cell buffer EN_n is switched ON during readout of the cell located b places before, and turned off during readout of the cell located f places after. This mechanism ensures that only $b+f$ cells are ON at the same time. b and f are hardwired so they have a fixed value, but could be made variable with the use of switches.

The selection of b is related to the settling time of the control signal, such as a bias voltage, and the turn-on time of the buffers, so it must be selected carefully to make sure that the buffer is fully operating at the time of readout, but that is not high enough that there are too many buffers turned ON at the same time. The optimal b and f for a certain implementation are functions of the operating voltage, frequency and temperature.

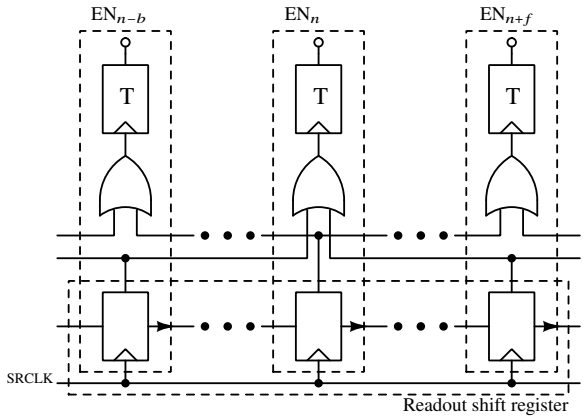

Fig 2 *Power cycling block diagram, where b and f are typically hardwired, thus fixed.*

An SCA with a power cycling circuit was designed for a 180 nm CMOS process, composed of a single channel with 512 memory cells arranged in 16 banks of 32 each, a fast clock generated on-chip for acquisition, and a shift register with external clock for readout. This design is structured in banks with a single bias voltage generation circuit shared to every buffer in the bank, and switched on with an external signal that comes from the power cycling circuit.

Simulation results: A simulation of the readout is shown in Fig. 3, where every 32 cycles there is a transition of the active bank, but the bias circuit is switched ON one cycle before the bank change to make sure that the transient is over when the buffers are operating. It can be noted though that after the bank transition the active bias voltage has not settled yet, which could be avoided with a higher b.

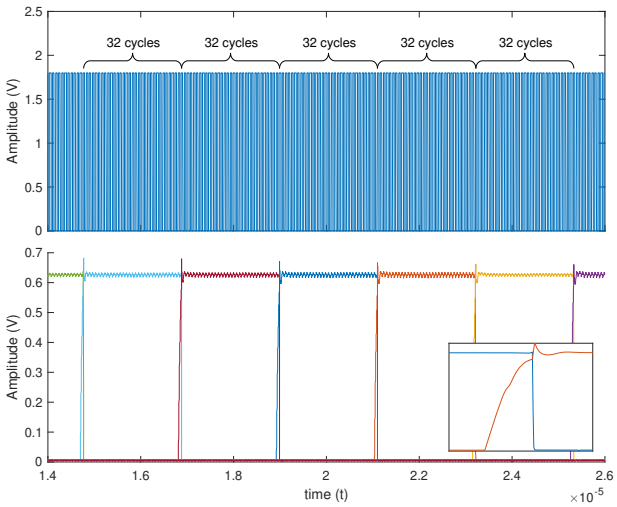

Fig 3 *Readout clock (top), banks bias voltages (bottom) and switch transient close-up (bottom right).*

Results show that the average power consumption of the complete chip during readout at 15 MHz was 18.4 mW. Without the effect of the power cycling, the value of the power consumption would have been 3.3 times larger at around 61 mW.

Conclusion: A power cycling circuit for readout buffers on SCAs was designed in this work. After being implemented in an SCA circuit design, the layout was fully extracted including parasitics and simulated, where it showed a decrease in total power consumption of about 3.3 times in comparison with always-on readout buffers, and this value could be improved even further for SCA circuits that allow individual control over cell bias voltages. A power cycling cell is about 2.8 times larger than a shift register cell, so a trade-off appears between a larger readout circuit and power consumption.

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