Design of capacitor-less LDO regulator with high reliability ESD protection circuit using analog switch structure for 5 V applications

Kwon Sang Wook[1], Koo Yong Seo[2]

[1,2] *Department of Electronics and Electrical Engineering Dankook University, 126 Jukjeon-dong, Gyeonggi-do, Republic of Korea*

Email: kso804@naver.com.

This letter suggests to the LDO regulator with the high reliability ESD protection circuit that achieves low peak voltage through analog switch structure. The proposed LDO regulator has the function of detecting the output voltage fluctuations depending on the load via an analog switch structure and effectively controlling the peak voltage. The proposed ESD protection circuit is placed on I / O and power lines to prevent the IC circuit from being destroyed from the inevitable ESD phenomenon. It was verified that the reliability of the IC can be improved through effective current discharge due to ESD surge. The proposed LDO regulator, implemented in a 0.18μm BCD process, achieves an undershoot voltage of 25 mV and an overshoot voltage of 28 mV for a load current of 300 mA.

Proposed LDO regulator with analog switch structure: The modern electronic device should be able to provide stable voltage and current under a variety of conditions. The LDO regulator used in the electronic device is a system that requires various voltages and load currents. Therefore, the LDO regulator must stably drive regardless of the change of load current [1, 2]. In addition, as ICs are miniaturized and integrated, circuit failures frequently occur in mobile devices using the low voltage due to electrostatic discharge (ESD). This is an important part of the impact on overall reliability, including productivity and reliability. To avoid this damage, it is important to improve the manufacturing environment and transport conditions of the IC, but the most important factor is to prevent external inflow and discharge of the ESD through ESD protection circuits built into the IC circuit. The LDO regulator proposed in this study designed an ESD protection circuit in the operating area suitable for low voltage applications and based on it has been confirmed to be robust to HBM 6kV or higher [4]. As a result, the proposed LDO regulator has configured an ESD protection circuit to ensure the high reliability. Figure 1 shows a block diagram of the proposed LDO regulator

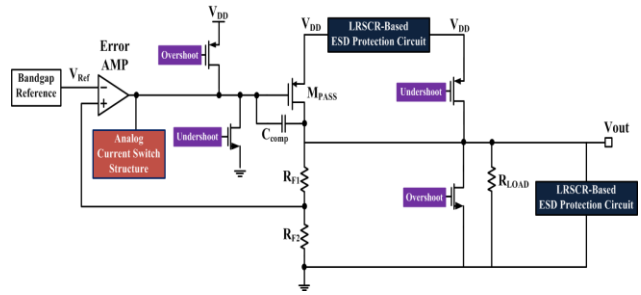

Fig 1 *Block diagram of the proposed LDO regulator using analog switch structure*

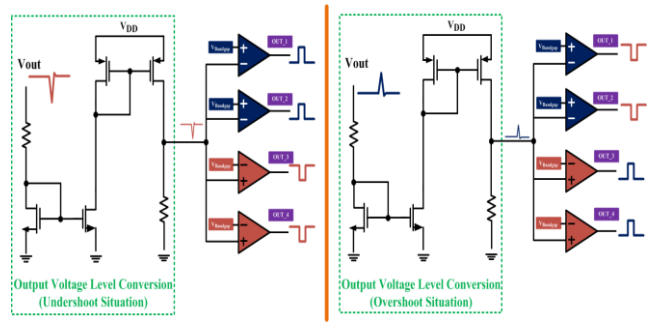

Fig 2 *Analog switch structure according to each situation*

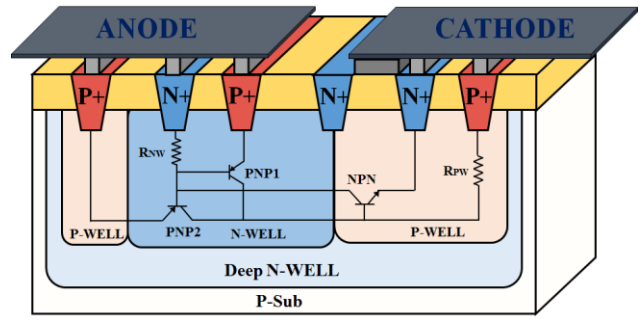

Fig 3 *LRSCR (Low Ron Silicon Control Rectifier)*

using an analog switch structure. Namely, it consists of an analog switch structure and a highly reliable ESD protection circuit. The momentary change of load current will affect the output voltage of the LDO regulator. LDO regulators must have a function to satisfy the various load current amounts. The proposed LDO regulator as shown in Figure 2 is input to the analog switch structure through output voltage level conversion, which can effectively control the output voltage with an analog switch structure in response to changes in load current. In the case of undershoot condition, a current is further discharged to the gate terminal of the pass transistor, and an additional current is supplied to the output stage to control the output voltage more effectively. Conversely, in overshoot situations, the gate terminal of the pass transistor is supplied with additional current, and the output stage discharges the additional current to effectively control the output voltage [3].

Proposed ESD protection circuit with LRSCR structure: According to Figure 3, the proposed LRSCR-based ESD protection circuit introduces a ground gate NMOS (GGNMOS) to lower the trigger voltage by causing the avalanche breakdown at the N-well and P-well junctions of the existing SCR to occur between the N+ diffusion

and P-well regions. The second parasitic PNP BJT (PNP2) is also operated in parallel through an additional P+ diffusion region (anode)/P-well/P+ diffusion region (cathode). Because PNP2 discharges ESD current by forming an additional parallel discharge path, the on-resistance is reduced and the robustness is increased [4-8].

Result and discussion: The proposed LDO regulator are designed with 0.18μm BCD process and its chip size is 510 × 462μm as shown in Figure 4. The analog switch structure has a function of effectively controlling the peak voltage by turning on/off the required current depending on the load. In addition, the proposed ESD protection circuit was configured and verified to effectively discharge the ESD surges in the mobile devices using the low voltage. Figures 5 and 6 are the results of measuring the transient response characteristics and the load regulation of the proposed LDO regulator. The proposed LDO regulator is effectively improved by adding a function to turn the current on/off using an analog switch to the peak voltage caused by the load current. When the load current is applied up to 300 mA, an undershoot voltage of 25 mV and an overshoot voltage of 28 mV were secured. As a result, it was verified that the analog switch structure of the proposed LDO regulator forms a system that could turn on/off a current additionally except for the existing current path and effectively controls the power voltage. Also, the LDO regulator using the analog switch structure ensured a change in the power voltage of 7 mV in the load current range of 0 to 300 mA. Figure 7 shows the result of measuring the quiescent current generated by the proposed LDO regulator. The quiescent current is a major variable that affects the performance of battery powered devices. A large quiescent current means that power is consumed continuously even when the device is not operating. It was confirmed that the proposed LDO regulator consumes 41μA of the quiescent current. And also, the proposed ESD protection circuit is designed to fit the ESD design window for applications using 5V by increasing the holding voltage to 5.98V. Thereby, it was confirmed that the proposed ESD protection circuit maintains lower trigger voltage, higher holding voltage, higher robustness, and lower ON resistance compared to the conventional SCR as shown in Figure 8. As a result, the proposed ESD protection circuit can discharge current more efficiently than conventional SCRs due to the larger current-driving capacity in applications using a 5-volt power clamp.

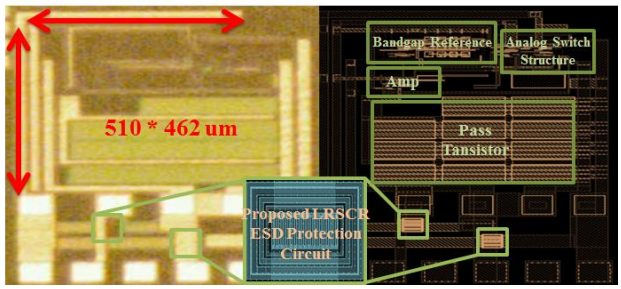

Fig 4 *Chip layout of analog switch structure LDO regulator including ESD protection circuit*

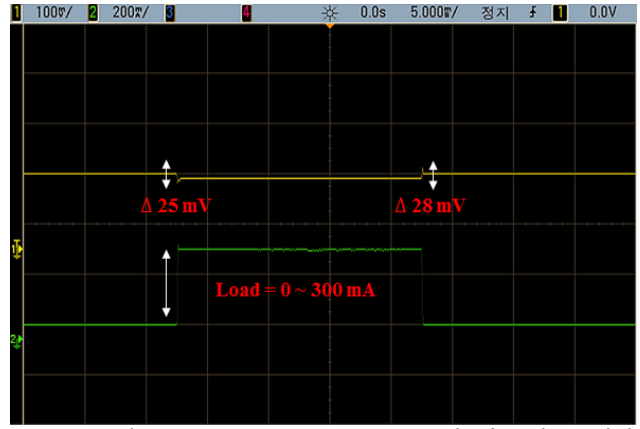

Fig 5 *Transient response measurement result of analog switch structure LDO regulator*

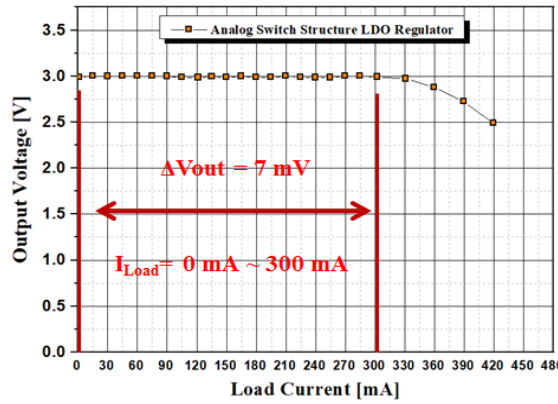

Fig 6 *Load regulation measurement result of analog switch structure LDO regulator*

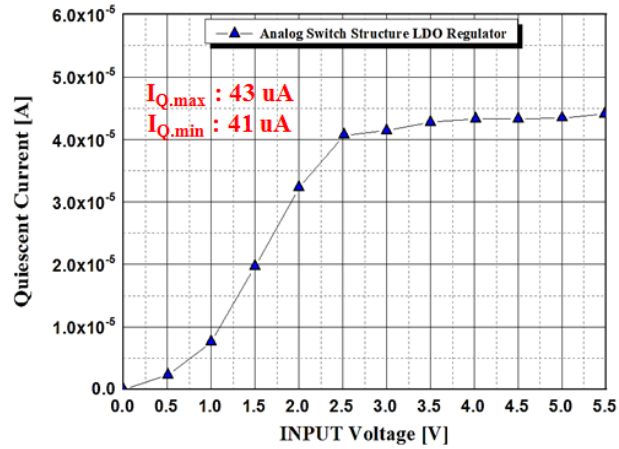

Fig 7 *Quiescent current measurement result of analog switch structure LDO regulator*

Therefore, the proposed ESD protection circuit has improved high reliability of 5V applications. Figure 9 measures and validates the thermal reliability of the proposed ESD protection circuit at high temperatures (300-500K). According to the measurement results, the proposed LRSCR at a high temperature of 500K has a maintenance voltage of 5.2V.

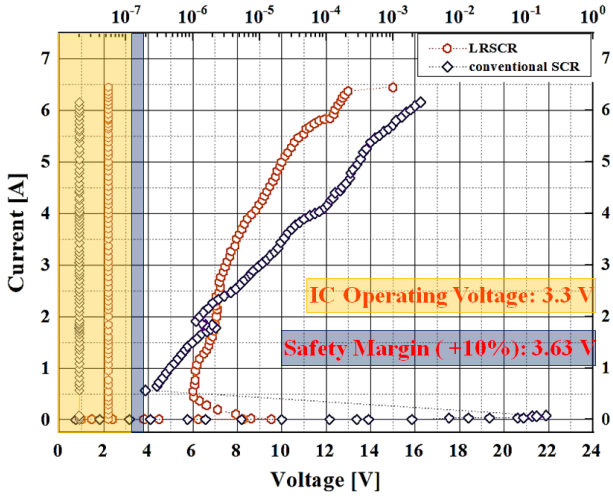

Fig 8 *TLP I–V characteristic of proposed ESD protection circuit*

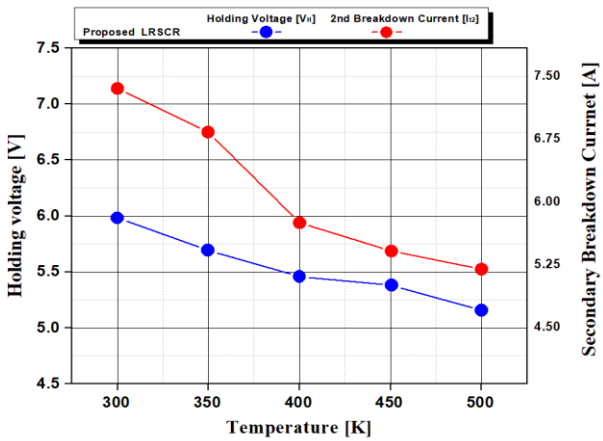

Fig 9 *High temperature (300-500K) electrical characteristics*

and the secondary trigger current is still high at 5.25A, which shows the high tolerance characteristics of the proposed circuit. Therefore, the proposed ESD protection element has excellent thermal reliability and high temperature characteristics.

Conclusion: The LDO regulators frequently used in the mobile devices must provide a linear voltage not only for a stable voltage, but also for the external ESD situations and the various load currents. The proposed LDO regulator using an analog switch structure is designed to have a system that can additionally turn the current on/off, including the existing current path. According to the measurement results, the proposed LDO regulator ensured an undershoot voltage of 25 mV and an overshoot voltage of 28 mV, even with a large load current of 300 mA. It was verified that the output voltage is effective in making it insensitive to changes in a large load current. Furthermore, the proposed high-reliability ESD protection circuit optimizes effective IC protection in low-voltage devices. As a result, the proposed LDO regulator was verified to ensure stable power voltage even at large load currents and high reliability of IC even in ESD situations.

Acknowledgments:

Received: xx January 2021 *Accepted:* xx March 2021
doi: 10.1049/ell2.10001

References

1. Yan Lu, Cheng Li, Yan Zhu, Mo Huang, Seng-Pan U, Rui P. Martins: A 312 ps response-time LDO with enhanced super source follower in 28 nm CMOS, Electronics Letters 52 (16), 1368–1370 (2016). https://doi.org/10.1049/el.2016.1719
2. J. Pérez-Bailón, A. Márquez,B. Calvo,N. Medrano,P.A. Martínez: Fast-transient high-performance 0.18 µm CMOS LDO for battery-powered systems, Electronics Letters 52 (16), 551-552 (2017). https://doi.org/10.1049/el.2016.1719
3. J. Hinojo, C. Luján-Martínez, A. Torralba: LDO compensation with variable Miller series resistance, Electronics Letters 50 (3), 159 - 161 (2014). https://doi.org/10.1049/el.2013.3450
4. Bo-Bae Song, Yong Seo Koo: Low Ron and high robustness ESD protection design for low-voltage power clamp application, Electronics Letters 52(18), 1554 - 1555 (2016). https://doi.org/10.1049/el.2016.2391
5. Kyoung-Il Do, Jong-Il Won, Yong-Seo Koo: A 4H-SiC MOSFET-Based ESD Protection With Improved Snapback Characteristics for High-Voltage Applications, IEEE Transactions on Power Electronics 36(5), 4921 - 4926 (2020). 10.1109/TPEL.2020.3032917
6. Kyoung-Il Do, Bo-Bae Song, Yong Seo Koo: A Gate-Grounded NMOS-Based Dual-Directional ESD Protection With High Holding Voltage for 12V Application, IEEE Transactions on Device and Materials Reliability 20 (4), 716 - 722 (2020). 10.1109/TDMR.2020.3022897
7. Kyoung-Il Do, Yong Seo Koo: A Novel Low Dynamic Resistance Dual-Directional SCR With High Holding Voltage for 12 V Applications, IEEE Journal of the Electron Devices Society 8, 635 - 639 (2020). 10.1109/JEDS.2020.2999108
8. Kyoung-Il Do, Seung-Hoo Jin, Byung-Seok Lee, Yong-Seo Koo: 4H-SiC-Based ESD Protection Design With Optimization of Segmented LIGBT for High-Voltage Applications, IEEE Journal of the Electron Devices Society 9, 1017 - 1023 (2021). 10.1109/JEDS.2021.3121212