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Mach-Zehnder Interferometer

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Abstract This report describes the design of Mach-Zehnder Interferometer, including its design background, components used, and physical parameters.

1 Introduction

(LaTeX version)

The Mach-Zehnder Interferometer (MZI) design is widely used in Photonics circuit. It can be used as photonics switches in data center. In this MZI design, y$_s$*plittersareusedatinputandoutputofthewaveguidetosplitthelightatinputand*c

$$\beta_{1,2} = \frac{2\pi\left(n + \frac{dn}{dt}\Delta T_{1,2}\right)}{\lambda}$$

*atoutput.A*50*um*/80*umwaveguid*

2 Theory

For a Y_splitter and combiner, the input intensity I_i Electric field E_i can be discribed as following:

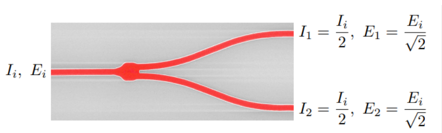

Fig. 1 Y_splitter

In MZI the intensity is [1]:

I_o = I_i x 1 / 2 x (1 + cos(β[?]L)

from the equation above, we know the length difference between 2 arms affect the output intensity of MZI design[2], also

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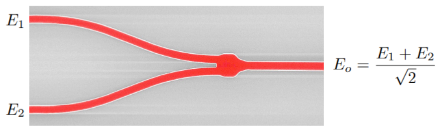

Fig. 2 Y Combiner

from the equation above, we know that the intensity also depends on the tempurature on the waveguide.

The FSR of MZI[3] is inverse proportional to length offset between two arms and group index.

$$\mathrm{FSR} = \Delta\lambda = \frac{\lambda^2}{\Delta L\left(n - \lambda\frac{dn}{d\lambda}\right)} = \frac{\lambda^2}{\Delta L n_g}$$

3 Modelling and Simulation

3.1

3.2 A. Waveguide:

In this design, we are using waveguide with 220nm in height, and 350nm in width. In layout, the width of waveguide and length offset between two arms can be updated as needed for different testing purpose.

the simulated waveguide mode profiles are the following:

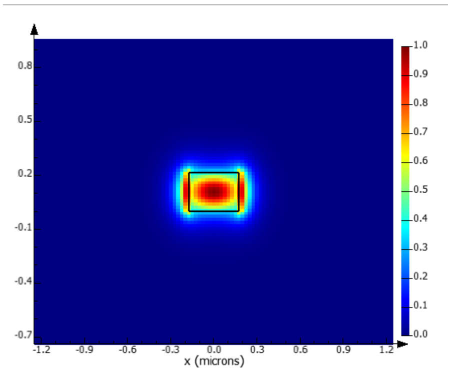

Fig. 3 Electric field intensity of TE mode in waveguide

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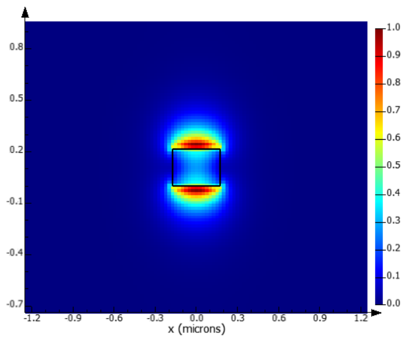

Fig. 4 Electric Field intensity of TM mode

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5.1 B. Mach-Zehnder Interferometer

INTERCONNECT software is used to model MZI performance.

A 50um lengh is introduced between two arms of 350nm waveguide. and grating coupler is used at input of the model. In this test case, the interference at MZI output is only affect by the length mismatch.

here is a TE gain plot of MZI:

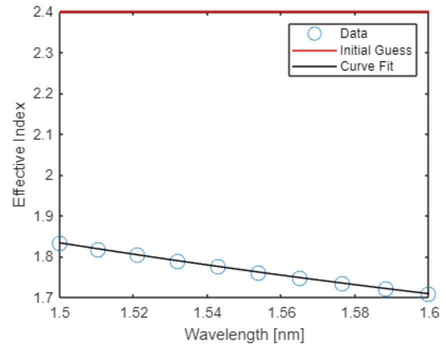

Fig. 5 effective index in TE mode

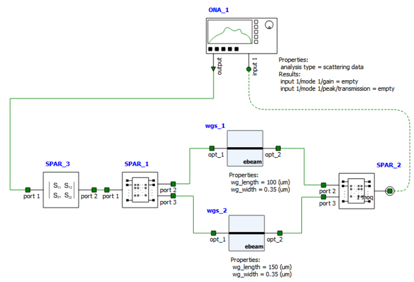

Fig. 6 INTERCONNECT MZI model

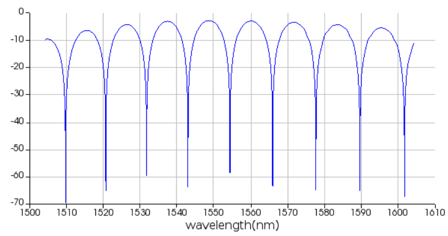

Fig. 7 TE gain of MZI

5.2 C. Design Variance

Silicon manufacturing variance occurs during fabrication. thickness and width of waveguide are not at 350nm or 500nm at this case, corner analysis is used in Lumerical to get max and min value of group index for 500nm waveguide.

the corners are thickness varies between 215.3nm and 223.1nm, width varies between 470nm to 510nm.[4]

Using those corners, we can get the minimum group index value is 4.17, and maximum group index value is 4.25 at TE mode.

5.3 D. IPKISS Design4

MZI layout are designed and simulated using ipkiss software. 5 difference MZI variances are designed. two of them have waveguide jog in order to study the manufacturing variances with longer waveguide.

Here is a table of design details:

waveguide width(nm)	waveguide length offset(um)	waveguide jog
0.5	80	yes
0.5	80	no
0.5	50	no
0.35	50	no
0.35	50	yes

Table 1 design variances

5.4 E. Simulation results

Each of those design were simulated using ipkiss after generated GDS.

Here are the plots of transmission vs. Wavelength on each design:

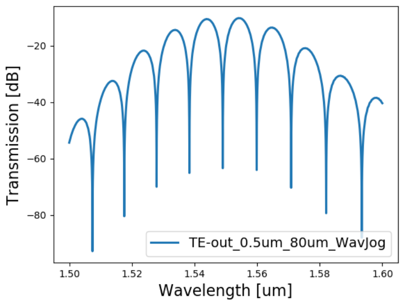

Fig. 8 0.5nm waveguide width 80um offset length with waveguide jog.

The waveguide jog affects the length of MZI waveguide and created more turns which results in lower transmission power.

Lower offset length have a bigger SFR.

thiner waveguide width have lower group index, and have a lower transmission power in MZI.

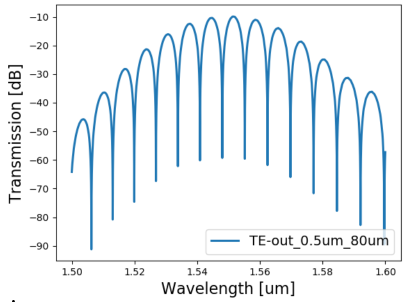

Fig. 9 0.5nm waveguide width 80um offset length without waveguide jog.

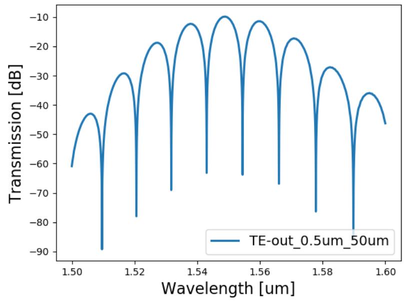

Fig. 10 0.5nm waveguide width 50um offset length without waveguide jog

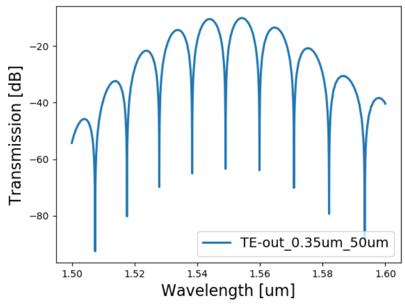

Fig. 11 0.35nm waveguide width 50um offset length without waveguide jog

6 Layout and Fabrication

The devices were fabricated using 100 keV Electron Beam Lithography. The fabrication used silicon-on-insulator wafer with 220 nm thick silicon on 3 μm thick silicon dioxide. The substrates were 25 mm squares diced from 150 mm wafers. [1]

Layout of MZI is designed using ipkiss, and GDS is viewed in KLayout.

Here is a snap shot of MZI layout:

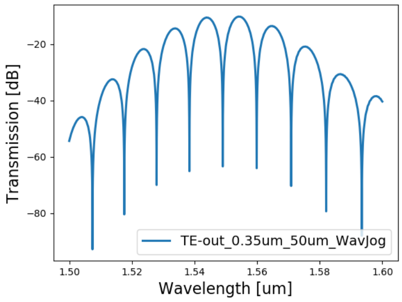

Fig. 12 0.35nm waveguide width 50um offset length with waveguide jog

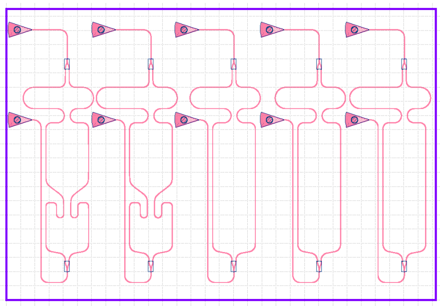

Fig. 13 MZI layout

All waveguide have thickness of 220nm, and width of 0.5um and 0.35um, tapers from SiEPIC_EBeam_PDK are used from transition with different waveguide width.

The following components are used from SiEPIC_EBeam_PDK as well:

1. Grating couplers : ebeam_gc_te_1550
2. Y-branch: ebeam_y_1550

All waveguide bends are manhattan bend in ipkiss with radius of 5um.

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8 5 Test Results

FRS and transmission power is simliar as simulated number, the waveguide jog did not have big impact on performance.

Minor differences between 0.35um and 0.5um waveguide width in testing data.

Group index and FSR are calculated using corners explained in section 3.3

The table below shows the calculated group index and FSR range compare to testing values:

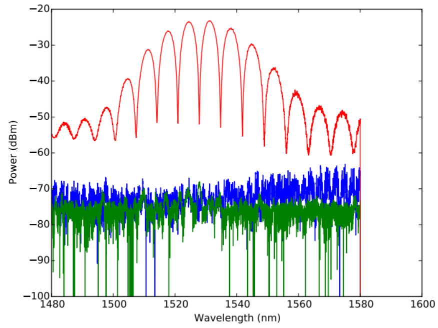

Fig. 14 0.5um width, 80um offset, with waveguide jog

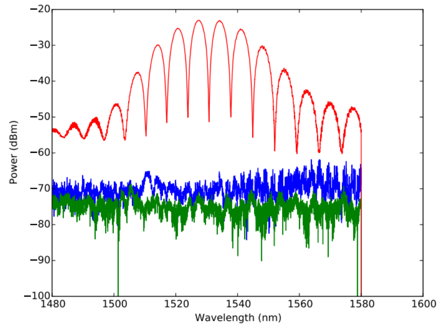

Fig. 15 0.5um width, 80um offset, without waveguide jog

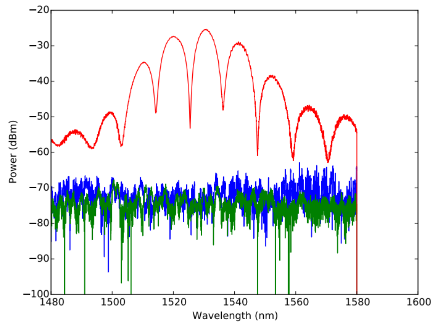

Fig. 16 0.5um width, 50um offset, without waveguide jog

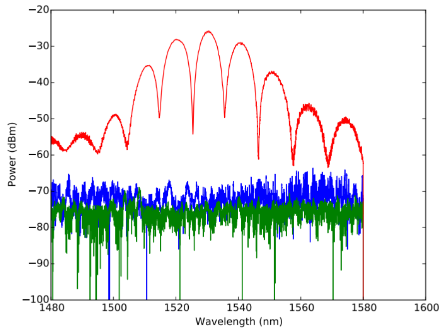

Fig. 17 0.35um width, 50um offset without waveguide jog

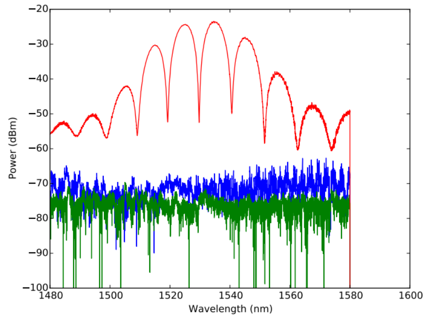

Fig. 18 0.35um width, 50um offset, with waveguide jog.

MZI model	group index	FSR	group index measured	FSR measured
0.5um width 50um offset	4.17-4.25	11.3-11.52	4.28	11.22
0.5um width 80 offset	4.17-4.25	7.06-7.2	4.21	7.13
0.5um width 80 offset with waveguide jog	4.17-4.25	7.06-7.2	4.2	7.13

The waveguide jog did not affect much of the group index and FSR which means the longer waveguide duing fabrication did not affect much of the performance.

9 5 Acknowledgements:

I acknowledge the edX UBCx Silicon Photonics Design course for all the information provided. Thanks to professor Lukas Chrostowski from UBC for putting together this outstanding course, and thanks to Iman Taghavi for helping with testing my design.

10 Reference

[1] Lukas Chrostowski, Michael Hochberg, “Silicon Photonics Design: From Devices to Systems”, Cambridge University Press, 2020

[2] Lukas Chrostowski, Michael Hochberg, “Silicon Photonics Design: From Devices to Systems”, Cambridge University Press, 2020

[3] Lukas Chrostowski, Michael Hochberg, “Silicon Photonics Design: From Devices to Systems”, Cambridge University Press, 2020

[4] Lukas Chrostowski, Michael Hochberg, “Silicon Photonics Design: From Devices to Systems”, Cambridge University Press, 2020