Modeling of High Roll-off SIW Coax Filter with Novel Coupling Structures and Stopband Transmission Reduction Methods

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Abstract
Proposed dual-mode substrate integrated waveguide (SIW) short-circuited coax filter demonstrates a passband that has transmission zeros on both upper and lower stopbands; in addition, such a filter is also inherent with good out-of-band rejection up to three times of the center frequency (f_c). There are four signal paths from input port to output port. The signal routings are done by conductor-backed coplanar waveguide (CBCPW) and the slotlines on the top metal. In addition to signal routings, frequency control capacitors (C_{Freq}), and electric coupling capacitors (C_E) are on the bottom metal. The center frequency of the passband can be determined by C_{Freq}, and the transmission zero on the lower-end can be tuned by C_E respectively. The phase delay of the signal routings are investigated individually as a way to explain the generation of the transmission zero below the passband. Furthermore, capacitors' touchstone files from the vendor are implemented in the schematic such that simulation results including all the parasitic components can be emulated to real-world measurements. In the best scenario, presented filter shows a prescribed passband centered at 4.84 GHz, and with insertion loss (IL) of 2.11 dB as well as 3-dB bandwidth of 0.46 GHz.

1. INTRODUCTION

In recent researches, the reports of bandpass filter design with multiple transmission zeros (TZ) on two sides of the passband are increasing. As the TZs move closer to the passbands, the passband roll-off can be greatly improved. While there are several techniques to introduce TZs to the transfer function, such as deploying none-resonate nodes (NRN) [1], mixed electric-magnetic couplings [2], cross couplings [3]-[5], and bandpass-bandstop cascade [6]-[9], many designs that claim to have multiple TZs also suffer dwindled spurious-free range [10]-[14], such as twice the center frequency (f_c) or less. In those designs, usually unwanted transmission near the passband can be observed. In contrast, in the proposed design, we demonstrate a dual-mode compact short-circuited coax (SCC) filter which has targeted center frequency at 4.84 GHz with out-of-band rejection better than 30 dB up to $3f_c$. Such a filter also has predefined notches on two sides of the passband. However, spurious-free range are limited with designs that use SCC resonator, given that the higher resonance modes introduce spurious transmission at higher spectrum.

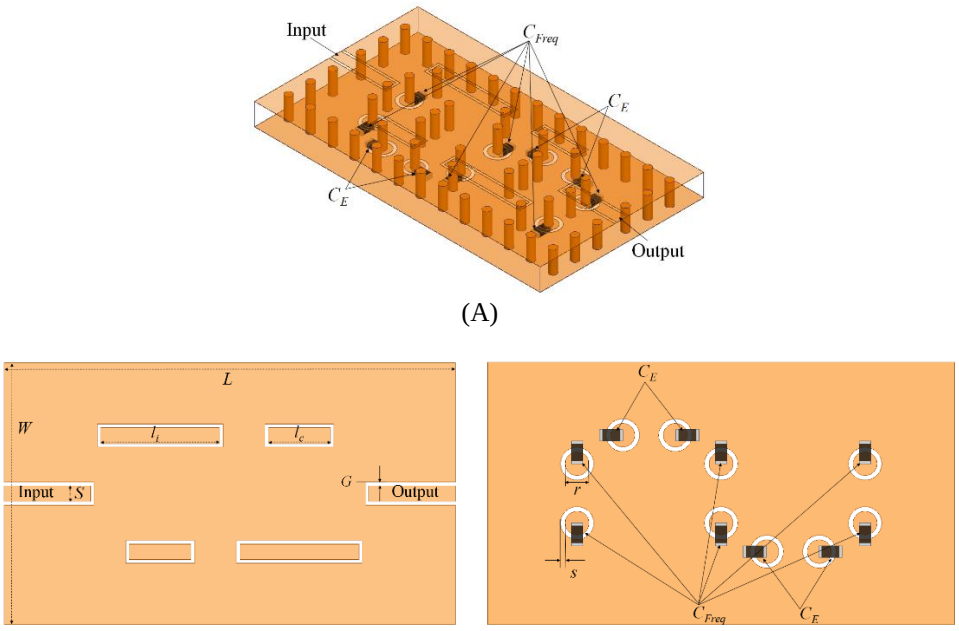


FIGURE 1 A, filter layout; B, top view; and C, bottom view

Thus compared with our previous design that used direct coupling scheme, in this paper, a novel side-coupling scheme is devised to reduce the level of unwanted spurs at higher frequencies. In addition, given that the surface mount technology (SMT) capacitors are none ideal but lossy, real capacitors' s2p files are later used to predict the performance of the filter, such that the in-band loss as well as the stopband rejection can be accurately characterized. Moreover, using multiple SMT capacitors in parallel to replace single standalone capacitor to better off quality factor and minimize parasitic inductance such that improve insertion loss and out-of-band rejection is also investigated.

2. DESIGN IMPLEMENTATION

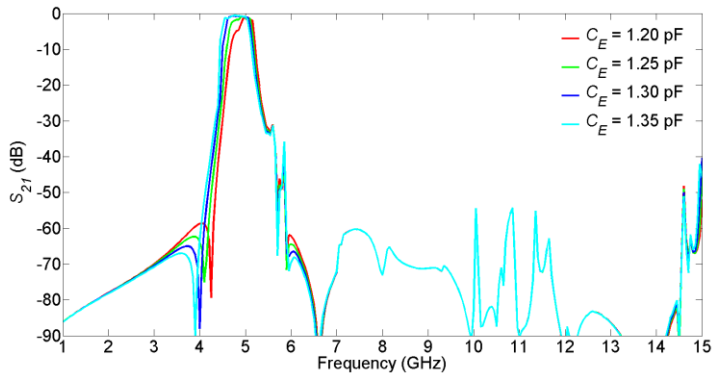
To begin with, the dual-mode resonator design for this filter can be found in [6]. Although it is possible to use two different capacitive loadings in each resonator to create dual passbands, throughout the paper only the design uses the same capacitive loading for each resonator is discussed. Based on three cascaded dual-mode resonators from FIGURE 8 from [6], a variant of such a filter is redesigned and shown in FIGURE 1. The critical dimensions of the filter are shown in TABLE 1. Compared to the design from [6] that has main signal path in the middle, the signal path in the middle is removed in this design; instead, the signal path is diverted to the sides, and forming two main signal routes. The lower arm and the upper arm are exactly the same but 180 degree mirrored from each other. Each contains two sets of slotlines, one set is short-circuited with the vias, and another set is terminated with SMT capacitors on the backside of the metal. Given that the magnetic coupling is dominant with short-circuited slotlines, the electric coupling is dominant with slotlines that has open-end on the backside. FIGURE 2 (a) reveals the frequency response versus C_E of the designed filter when C_{Freq} = 1.0 pF. In ANSYS High Frequency Structure Simulator (HFSS) model, the input and the output are set as wave ports, and each capacitive loading

TABLE 1 Filter Dimensions

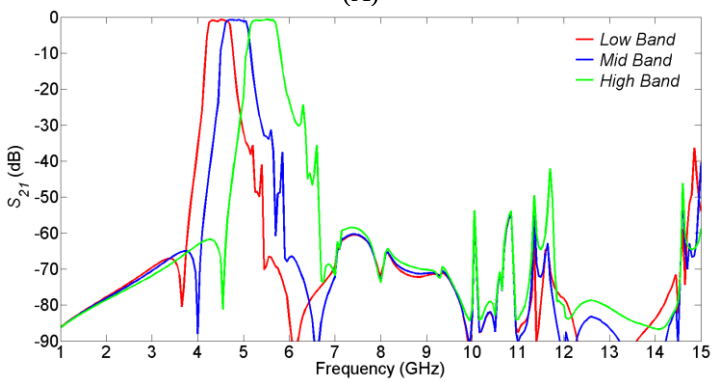
Parameters	W	L	H	S	G	l_i	l_c	r	s
mm	11.5	20.1	1.524	0.70	0.15	5.3	2.76	0.52	0.2

is set as lumped port, and later in Advance Design System (ADS) bench such a lumped port can be assigned to a capacitor which is shorted to ground at the one end. While all capacitors are assumed ideal, they have consistent capacitance, zero parasitic inductance, as well as zero parasitic resistance over the frequency. Since all the capacitors are assumed ideal, the IL of the passband is low; moreover, the out-of-band rejection is better than -40 dB up to 3 f_c. FIGURE. 2 (b) demonstrate three bands of the filter can be individually configured with different sets of ideal C_{Freq} and C_E applied. When ideal capacitors are used, some spikes are observed near the upper-end skirt, but such spurs are of little concerns when real capacitors are used due to the parasitic resistance of the capacitor will attenuate out those spurs. While only two signal routes are seemed to be implemented in the design, there are actually four routes. Shown in FIGURE 3 are each signal path of the filter. Since each path has different phase delay, the phase delay of each route can be separately plotted to understand how the transmission zeroes are obtained.

The phase of S_{21} of each path is studied and illustrated in FIGURE 4. Since route 1 is the reverse of route 3, it is no surprised that the phase delay of both routes are identical. When the phase delta reaches to 180 degree, transmission of the signal is ceased; consequently, transmission zero can be obtained at certain frequencies. When C_E is increased, the cross-point of the phase delay of route 2 and route 4 is relocated to the lower frequency, and such a phase is almost 180 degree deviates from the phase of route 1 and route 2.



(A)



(B)

FIGURE 2 A, C_E sweep while C_{Freq} = 1.0 pF; B, low-band: C_{Freq} = 1.2 pF, C_E = 1.55 pF; mid-band: C_{Freq} = 1.0 pF, C_E = 1.30 pF; high-band: C_{Freq} = 0.75 pF, C_E = 1.05 pF

For example, when C_E = 1.30 pF, the cross-point of phase delay of route 2 and route 4 is 3.94 GHz, and the corresponding phase delta to route 1 and route 3 at this particular frequency is 175.10 degrees. When the phase difference reaches to 180 degrees at a particular frequency, transmission of the signal is completely ceased; consequently, transmission zero can be obtained. TABLE 2 shows the cross-point frequency f_{cross} and the corresponding lower-end transmission zero frequency f_{LTZ} versus changes of C_E. As C_E increases, both f_{cross} and f_{LTZ} decrease; thereby, the lower-end notch is reconfigured to the lower spectrum. After incorporating all four signal routes into a single design, a filter with zeros on both sides of the passband can be obtained due to the cancelling effect brought by the multipath signals. Furthermore, unlike the previous designed filter that used the direct-coupling scheme, the side-coupling scheme is adopted in this work. The direct-coupling scheme that proposed in the previous design has a drawback of narrowed spurious-free range due to current probes are placed near the center of each resonators and become very close to each other, therefore, energy can propagate through the structure at a higher frequency such as $2f_c$ or so. On the other hand, much wider spurious-free range can be realized by deploying the side-coupling scheme. Note that in previous work, noticeable unwanted transmission can be observed roughly at $2f_c$ whereas in this work, out-of-band rejection holds up well up to $3f_c$.

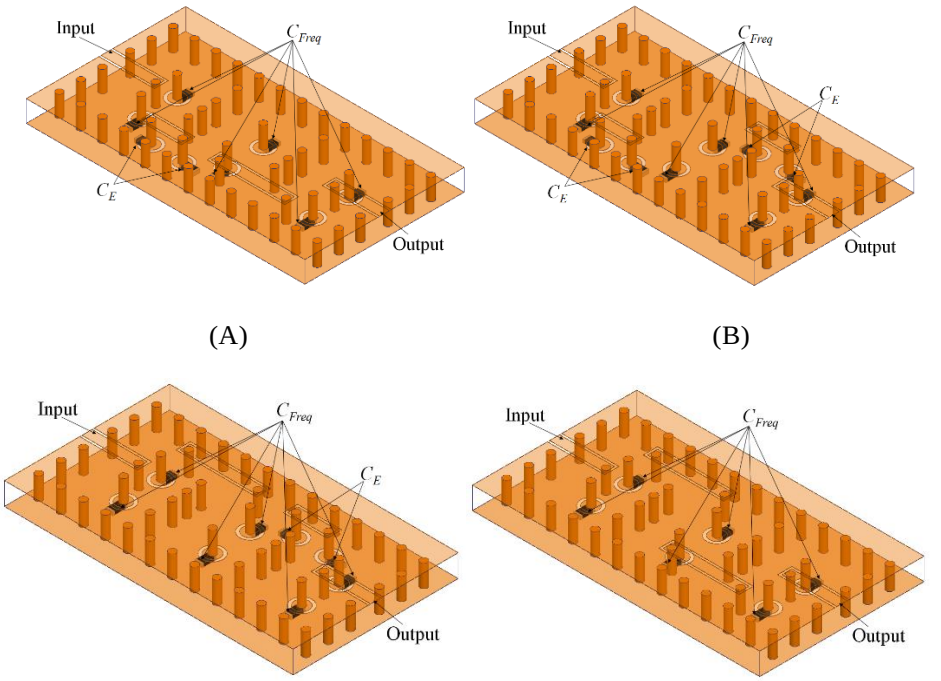


FIGURE 3 A, route 1; B, route 2; C, route 3; D, route 4

TABLE 2 Cross-point Frequency of Phase Delay of Route 2 and Route 4

	C_E = 1.20 pF	C_E = 1.25 pF	C_E = 1.30 pF	C_E = 1.35 pF
f_{cross} (GHz)	4.07	4.00	3.94	3.87
f_{LTZ} (GHz)	4.25	4.10	4.00	3.90

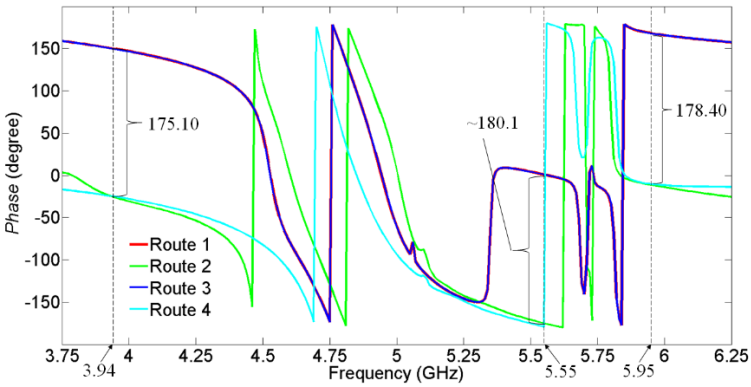


FIGURE 4 Phase and phase delta at TZs when C_{Freq} = 1.0 pF and C_E = 1.30 pF

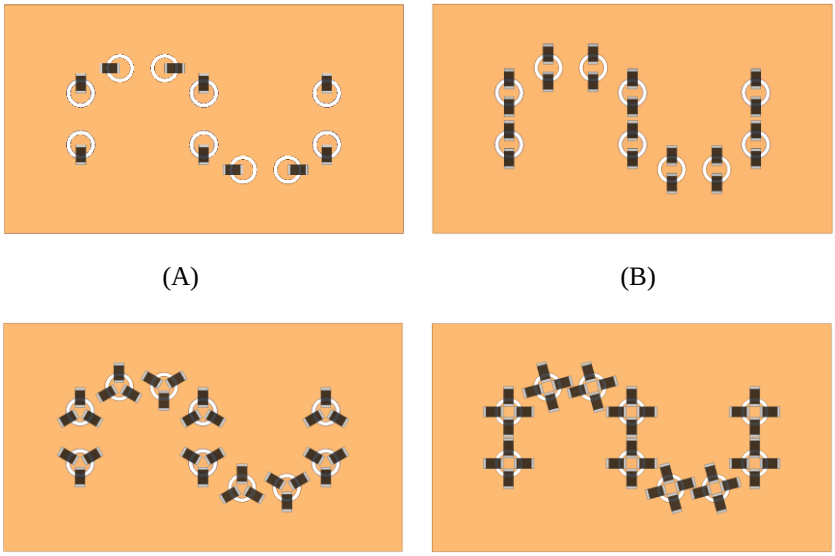
3. DESIGN IMPLEMENTATION WITH REAL CAPACITORS

By far, ideal capacitors that have consistent capacitance with zero equivalent series resistor (ESR) and zero equivalent series inductor (ESL) are used in the simulations. However, in reality, equivalent capacitance rises while the quality factor (Q) degrades with respect to frequency increase due to these parasitic elements take effects. According to [15], when multiple parallel capacitors are used, total ESR can be minimized thus improve the overall Q of the equivalent capacitor as a whole. Meanwhile, since the unloaded quality factor (Q_u) of a given capacitive-loaded SCC resonator heavily depends on the Q of the capacitor [6], improving overall Q of the capacitor results in better Q_u of the resonator. Conceptually, by deploying multiple smaller capacitors in parallel, the total ESR can be reduced. Borrowing the same idea, we further investigate how the ESL can be reduced in the similar fashion, given that the parasitic inductance can directly impact out-of-band transmission. In order to extract the ESR and ESL, one-port model of a series *RLC* is used, and when the S_{11} contour in the Smith chart from the equivalent circuits matches with the one from the s2p files from the vendor, the component values of the equivalent series *RLC* are recorded accordingly in TABLE 3. Equivalent capacitance and Q at 4.84 GHz are also calculated, where 4.84 GHz is the center frequency of the passband that serves as an example in the following section. Such a series *RLC* is later used in the ADS bench as a way to emulate the results derived directly from the real capacitors' touchstone files. In FIGURE 5, the schematic of the different capacitor configurations are shown.

TABLE 3 Extracted Capacitors' Equivalent Series *RLC* versus Capacitor Configurations

	Single	Dual	Triple	Quad
C_{Freq} / C_{Freq}' (pF)	0.75 / 1.02	0.85 / 1.01	0.90 / 1.01	0.90 / 0.99
ESC_{Freq} (pF)	0.755	0.854	0.90	0.920
ESR_{Freq} (Ohm)	0.350	0.250	0.250	0.250
ESL_{Freq} (nH)	0.385	0.199	0.132	0.110
Q_{Freq}	123.62	154.74	146.15	142.97
C_E / C_E' (pF)	0.90 / 1.29	1.05 / 1.30	1.10 / 1.28	1.15 / 1.29
ESC_E (pF)	0.90	1.05	1.10	1.15
ESR_E (Ohm)	0.250	0.20	0.19	0.185
ESL_E (nH)	0.362	0.196	0.12	0.105
Q_E	146.15	156.59	157.34	150.50

C_{Freq} is the labeled value of the capacitance, and can be regarded as an equivalent series circuit of ESC_{Freq}, ESR_{Freq}, and, ESL_{Freq} where C_{Freq}' is the extracted equivalent capacitance of C_{Freq} at 4.84 GHz; similarly, C_E is the labeled value of the capacitance, and can be regarded as an equivalent series circuit of ESC_E, ESR_E, and, ESL_E where C_E' is the extracted real capacitance of C_E at 4.84 GHz.



(A) (B)

(C) (D)

FIGURE 5 Capacitor configuration A, single; B, dual; C, triple; and D, quadruple

While it is possible to use different parallel capacitor combinations to yield the same equivalent capacitance, we try to use the ones that have similar labeled capacitance in each capacitive loading. Meantime, the extracted equivalent capacitance C_{Freq}' and C_E' of the designed capacitor groups needs to be aligned to 1.0 pF and 1.30 pF respectively at 4.84 GHz as TABLE 3 suggested, such that fair comparisons can be made. Shown in FIGURE 6 is how the capacitor implementation can be done in the ADS bench. In single capacitor configuration, each net connects to a single data item contains a s2p file from the capacitor; in quadruple capacitor configuration, each net connects to four data items. Later, the data items of the capacitors are replaced by series *RLC* shown in FIGURE 7. as a way to further investigate the cause of the out-of-band transmission.

In FIGURE 8 (A), the frequency response of the filter versus the capacitor's configuration is illustrated. The 0402 AVX Accu-P series capacitors' s2p touchstone file from the vendor are used in the simulation. With only one single capacitor used, the passband insertion loss is the highest, and the bandwidth is the least. While maintaining the total equivalent capacitance, the total ESR and ESL are reduced as the number of the parallel capacitor adds up. Thus, the equivalent quality factor of the capacitor increases, and such a capacitor has more consistent equivalent capacitance over the frequency due to the self-resonant frequency becomes higher as the parasitic inductance is reduced. When ideal capacitors are applied, the bandwidth is the largest with the least insertion loss due to the capacitor has infinite *Q* and constant capacitance versus frequency. Both the bandwidth and the in-band loss are the worst with the single real capacitor configuration because the single real capacitor configuration shows the largest ESR and the most inconsistent equivalent capacitance over the frequency due to the lower self-resonant frequency caused by the larger ESL. Moreover, the out-of-band transmission can also be mitigated with higher orders of the capacitor implemented given that the total ESL becomes less. By using extracted series *RLC* values from TABLE 3, FIGURE 8 (B) demonstrates the results from series *RLC* are well-correlated to the results derived from the capacitors' s2p files. Obviously, the high frequency spurs are strongly related to the ESL.

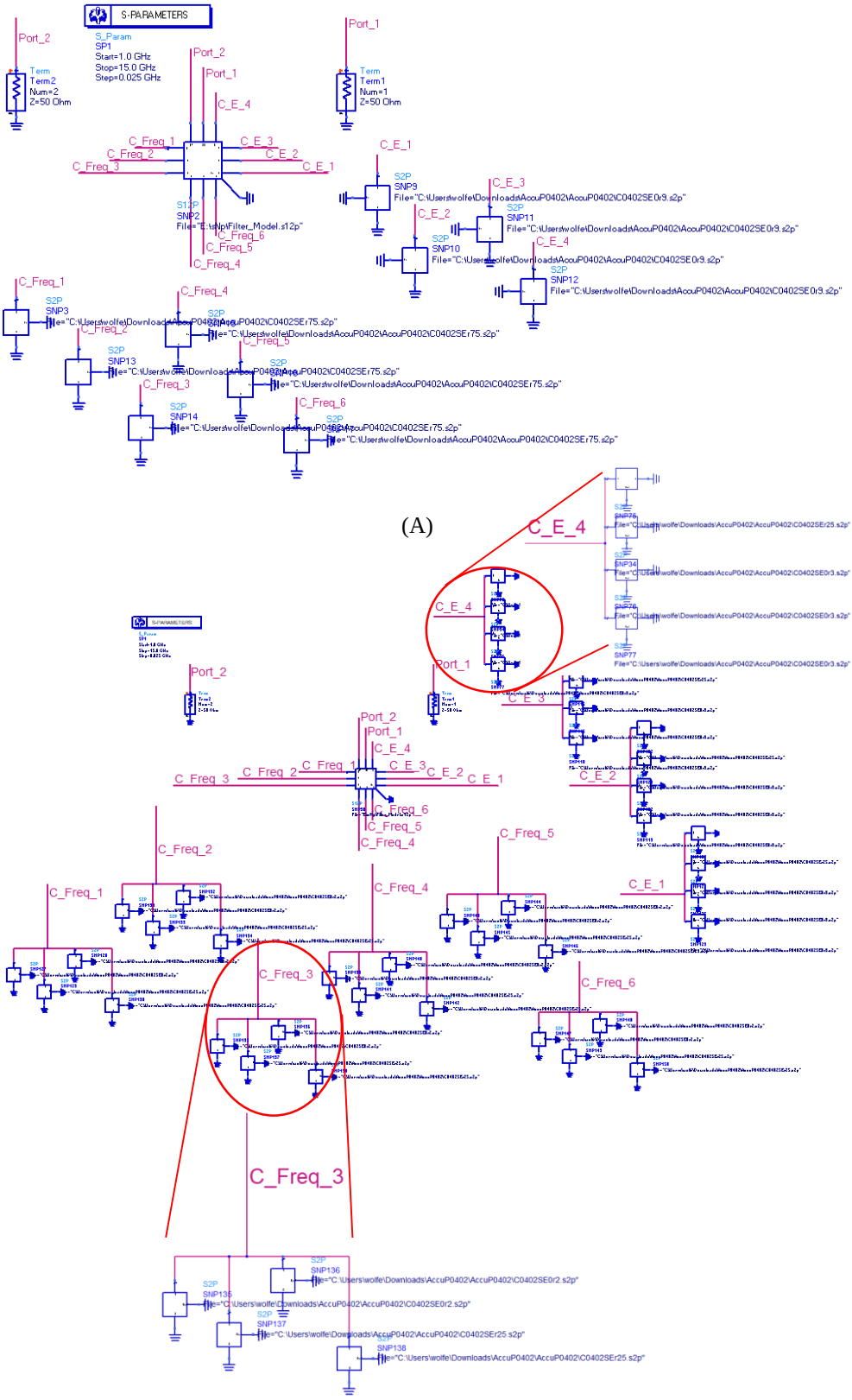
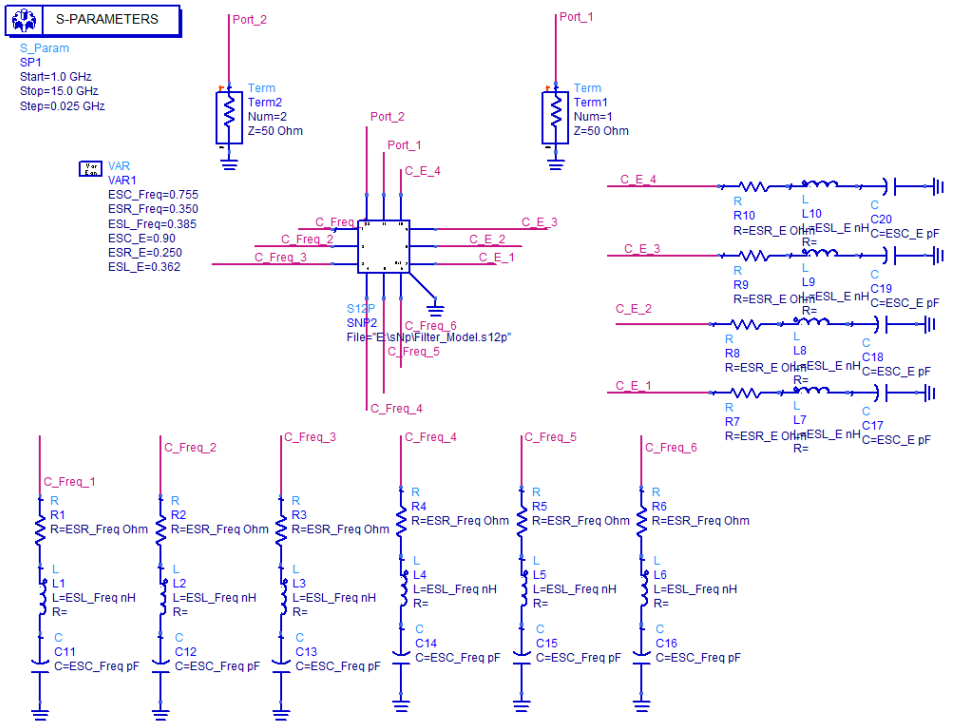
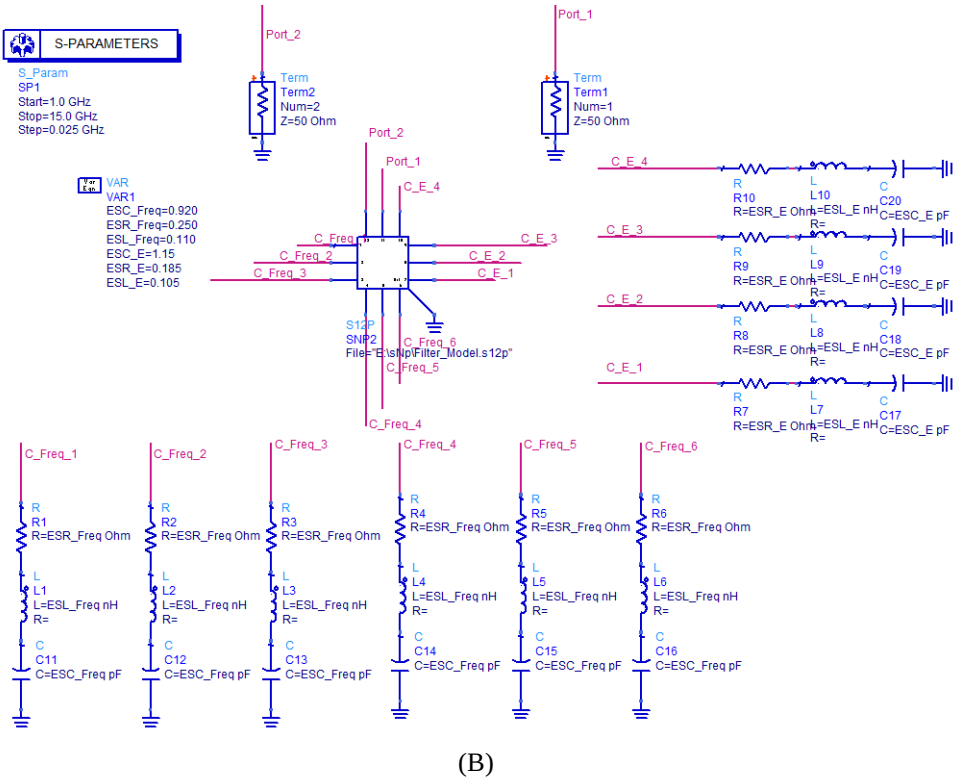


FIGURE 6 ADS bench configuration: A, single capacitor; B, quadruple capacitor

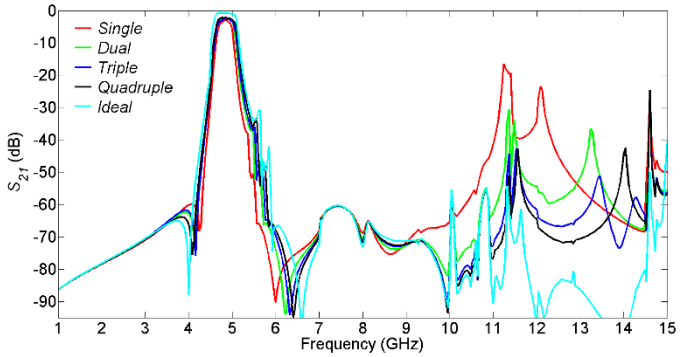


(A)

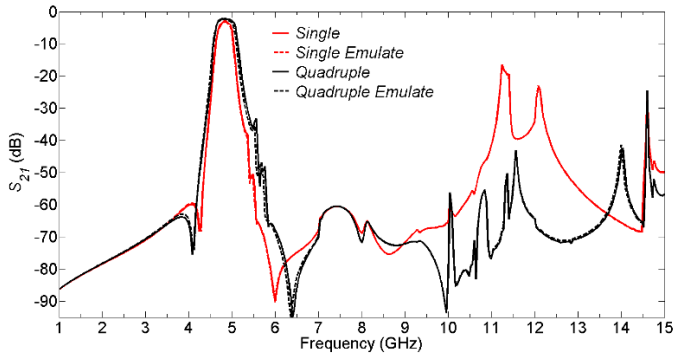


(B)

FIGURE 7 ADS bench: A, single capacitor configuration with extracted series *RLC*; B, quadruple capacitor configuration with extracted series *RLC*



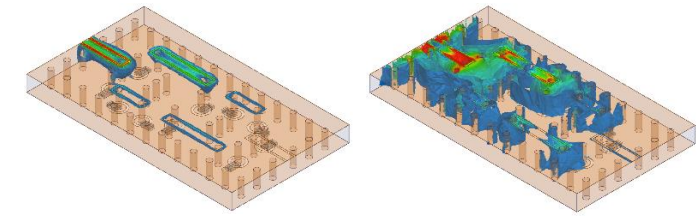
(A)



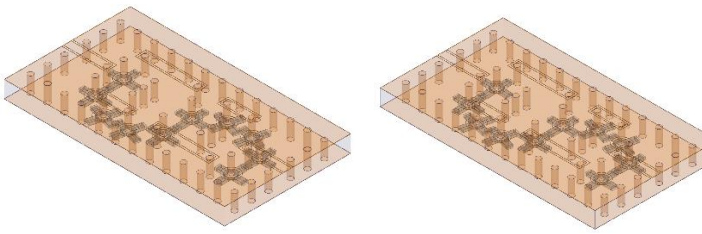
(B)

FIGURE 8 A, S_{21} versus capacitor configurations (simulated with capacitors' s2p files only); B, simulated results from s2p files (solid) versus results from series *RLC* (dotted)

A rapid-changing spike can be observed for all four configurations at 11.40 GHz. To verify how parasitic components are introducing the spike, the extracted series *RLC* value are then converted to parallel *RLC* at this particular frequency, such that the converted values can be set as lumped *RLC* boundary in HFSS model. FIGURE 9 shows the field plots comparisons between the two configurations at 11.40 GHz. With the single capacitor



(A) (B)



(C) (D)

FIGURE 9 field plots at 11.40 GHz: A, E-field of single capacitor configuration; B, H-field of single capacitor configuration; C, E-field of quadruple capacitor configuration; D, H-field of quadruple capacitor configuration

configuration applied, unwanted parasitic modes are excited inside the substrate and create transmissions; however, in quadruple capacitor configuration, no field can be observe due to the minimal transmission while the same plotting scale are applied. Needless to say, the main benefit of replacing single capacitor with multiple capacitors in parallel to suppress stopband spikes is evident.

4. CONCLUSION

In conclusion, proposed design demonstrates an alternative way to introduce zeros to the two sides of the passband. In general, good out-of-band rejection below -30 dB is extended to three times of the center frequency. By using the vendor provided capacitor's touchstone file, the performance of the filter can be accurately predicted. In addition, using multiple parallel capacitors to replace single standalone capacitor in each capacitive loading to reduce the overall ESR and ESL can improve in-band loss as well as suppress out-of-band spurs. Hence, it becomes more plausible for designing a short-circuited SIW coax bandpass filter that uses SMT capacitors as capacitive loads at higher frequencies. Last but not the least, proposed design can be easily integrated with other planar structures such as microstrip or coplanar waveguide, and the manufacturing cost of the single laminate PCB are comparatively low.

5. ACKNOWLEDGMENT

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