

FPAA-FPGA Architecture Noise reduction Analysis in the Front-End of the ALICE/ACORDE Experiments: Mixed-Mode design method.

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ABSTRACT: In this paper, the prototyping of an Mixed-mode architecture to reduce the noise effect in the front-end of the ALICE/ACORDE digital instruments is reported. It summarily portrays the design method implemented for configuration and reconfiguration of the proposed circuits by using Field Programmable Analog Array (FPAA) as the analogue channel and the FPGA as the adaptive digital subsystem. Their function was determined in the time domain using the original signal measured from the Front-end system. The data for the design were obtained from previous experiment developed at CERN Practical experimentation and the circuits was carried out using the AN221E04 FPAA device using Anadigm and Xilinx ISE interfaces. Circuit realization of improvement filter using hybrid architecture are shown in figures. Also, original input and result output waveform of implemented architectures are shown. A comparison of the proposed designed circuits with previous results published is also presented. The proposed scheme can be applied in the research and practical study of designing programmable analog devices and systems based on FPAA but the adaptive structure using FPGA.

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Nowadays, the novel electronic architectures can apply analogue and digital System on a Chip but there are not several real improvements applied in Recent Circular Colliders. The groundbreaking work of Graciós et al [?] on the modeling and control of Programable structures has found attention by the industrial community as a major advance. On the other hand, it is essential to consider that the use of the FP mixed strategies in the Instrumentation and control of High Energy Physics may be a great opportunity to develop and reach new challenges with the benefits of both design prototyping scheme. The last contribution by Jean [?], simple modification can be realized in mixed-mode integration design to obtain good results when analogue and digital systems are coupled. In addition, Roel et al [?] have demonstrated that the hybrid design platform is ready to evaluate and apply the traditional separated design architecture in just one SoC using FPAA as a primary design platform. At last, just a few mixed-mode implementation are been developed to reduce the implicated noise in front-end architecture in physical experiment such as ALICE/ACORDE experiments. This is the principal reason because this novel approach is relevant.

1 Fundamental Concepts

It is well-known that the novel High Energy Physics Experiments (HEPE) represents a great challenge in terms of the Design for Structural and Functional parametric detector behavior on Future Circular Collider (FCC). One of this particular aims is the low voltage power distribution to the front-end electronics embedded in this type of architectures [?].

Several constraints must to be considered and resolve taking into account the preliminary design for the whole instrumental and control schemes. The internal current from detectors must be more efficient in the distribution process for voltage regulation, power transmission lines and signal processing and filtering.

Accord with the evolution in IC technology, the design of this type of architectures can be improvement applying the nano-metric scales of integration between 130 to 65 nm CMOS by low-voltage low-power technique design [?].

The extremely high radiation levels within hadron collider (e.g. LHC and HLLHC) experiments will cause commercial nano-metrics devices to fail immediately"[?], either because of total dose

or because of radiation induced single event effects (e.g. single event burnout). Only dedicated and highly optimized power conversion components can survive in such an environment.

The active power conversion integrated circuits will have to stand relatively high voltages (10 V), but semiconductor technologies working at that voltage level, are unfortunately known to be particularly sensitive to radiation effects. Hence, significant dedicated HV IC technology radiation qualification work combined with detailed and specialized circuit and IC layout work is required to implement reliable data processing structures.

Several experimental front-end ASICs with built in shunt regulators have been successfully designed in the community and small-scale system tests have shown encouraging results [?].

These type of required ASICs can be design to process the signals associated at the Instrumentation and Control schemes for the Front-End devices inserted in the detectors for FCC considering the radiation effects described previously.

However, only, digital or analogue architectures can be found in recent detector but a mixed-mode strategy is quite new.

Finally for future experiments which aim to work with pulsed beams (e.g. ILC, CLIC, FCC), where the detectors only need to be sensitive for a fraction of the time, the use of adaptive and mixed-mode signal processing data is a very attractive option for minimizing the implicated noise and reduced the dissipated power inside the detector with Fast Computational Architectures (FCA) including the experiments high level restrictions.

Maintaining stable and low noise performance of the analogue parts of millions of multiple channels is a major challenge requiring significant R&D activities for both the front-end ASIC's and the global parameters distribution system in FCC and its components [?].

The architecture of the global power distribution system, the implementation and use of local power conversion techniques (on-module and/or on-chip) will have a major impact on the actual physics performance of many detectors (FCC). Here, the main reason to proposed the mixed-mode FPAA/FPGA architecture which let to develop an adaptive filter.

Then to extend the results of [?] including the improvement in the Front - End design reported in [?], the methodology described by Graciós et al is proposed[?].

Then this article analysis the adaptive filter solution explained in section 2. In Section 3 is described the structure and functional of the system designed. Finally, Section 4 discuss the results obtained in the experiment comparing with previous Front-end signals behavior. Section 5 is devoted for conclusions and future work.

2 Adaptive Filtering

According to Belloni [?] there exist several new requirements for the electronic applications. (See fig .1) These new requirements can be more exigent in terms of the level of applications schemes. This is the particular challenge area of High Physic Energy Instrumentation.

In the Future Circular Collider reports (www.tlep.web.cern.ch), recently, several improvements in Physics Instrumental have been developed, tested and applied considering some particular issues such as: Bandwidth (BW), Noise (S/R) and Low Voltage/Low Power (LV/LP) characteristics.

Nevertheless, some authors have reported the possibility to improve in other performance index of the dynamic measurements.

Some of this type of architecture have been designed, described and integrated considering one of the two design method; i, e, Analogue or Digital. However, if one of them is used for the whole integration system then it is possible to reduce the performance in other parameters.

In terms of Adaptive Filtering, several contributions have been made. Accord to [?] several type of algorithms are reported to achieve the new filter requirement. One of this type of parameters is the noise implication in design.

By this asseveration, it is desirable to obtained a more robust architecture which can accomplish the accurate level of parametric indexes for the complete design[?].

Obviously, these parameters must be measured with the adequate sensors to match in the design structure [?].

A way to improve the sensor measurements is by using smart-sensors which commonly perform self-adjusting, signal filtering, transducer resolution increasing, and fused parameters estimating functions. Furthermore, smart sensors are utilized to measure variables such as temperature, voltage and current, motion dynamics, kinematics, and many other derived variables such as Luminosity, and other physical variables[?].

Let $Ch_1(t)$ be the ACORDE Front-End Output signal, which can be divided in the addition of the $s_1(t)$ and its implicated noise $n_1(t)$, defined by:

$$Ch_1 = s_1(t) + n_1(t). \quad (2.1)$$

And let $Ch_2(t)$ for the processing channel in the output FPAA:

$$Ch_2(t) = s_2(t) + n_2(t)$$

Now, for any signal with delay:

$$y(t) = x(t - t_d) + n(t)$$

where t_d = delay time and $x(t)$ is the original signal and $y(t)$ is the signal with delay and noise signal then, the Cross Correlation can be defined by:

$$R_{yx}(\tau) = \lim_{T \rightarrow \infty} \int_{-T/2}^{T/2} y(t + \tau) x^*(t) dt$$

Considering $Ch_1(t) = x(t)$ and $Ch_2(t) = y(t)$ then the last expression is rewritten as:

$$R_{Ch_2(t)Ch_1(t)}(\tau) = \lim_{T \rightarrow \infty} \int_{-T/2}^{T/2} Ch_2(t + \tau) Ch_1(t) dt$$

Expanding for the delay time...

$$R_{Ch_2(t)Ch_1(t)}(\tau) = \lim_{T \rightarrow \infty} \frac{1}{T} \int_{-T/2}^{T/2} [Ch_1(t - t_d + \tau) + n(t + \tau)] Ch_1^*(t) dt$$

It implies:

$$R_{Ch_1(t)Ch_1(t)}(\tau) = R_{Ch_1Ch_1}(\tau - t_d) + R_{nCh_1(t)}(\tau)$$

If in any testing procedure with white noise added at the experimental approaching:

$$R_{uu}(\tau) = \frac{1}{2}$$

then the Autocorrelation is a constant value equal to 1/2, it is the spectral density of power is its Fourier transform itself. By this assumption, the autocorrelation by white noise definition can be used to evaluate the relationship between the two signals correlated by noise influence.

3 Mixed- Mode Architecture proposed

Mixed mode architecture proposed [?] is based on FPGA Altera Max II Development Kit which is embedded a dynamic PIC structure by FPAA prototyping board (See Fig. 2). The FPGA is used to describe the structure and function of the PIC in the FPAA board to modify the Switched Capacitor Frequency in closed-loop scheme. This whole architecture will function as an adaptive filter to reduce the noise in the ACORDE signal processing.

It is possible because the FPAA architecture processes the signal in analogue form and the digital conversion develop by the FPGA scheme is not required.

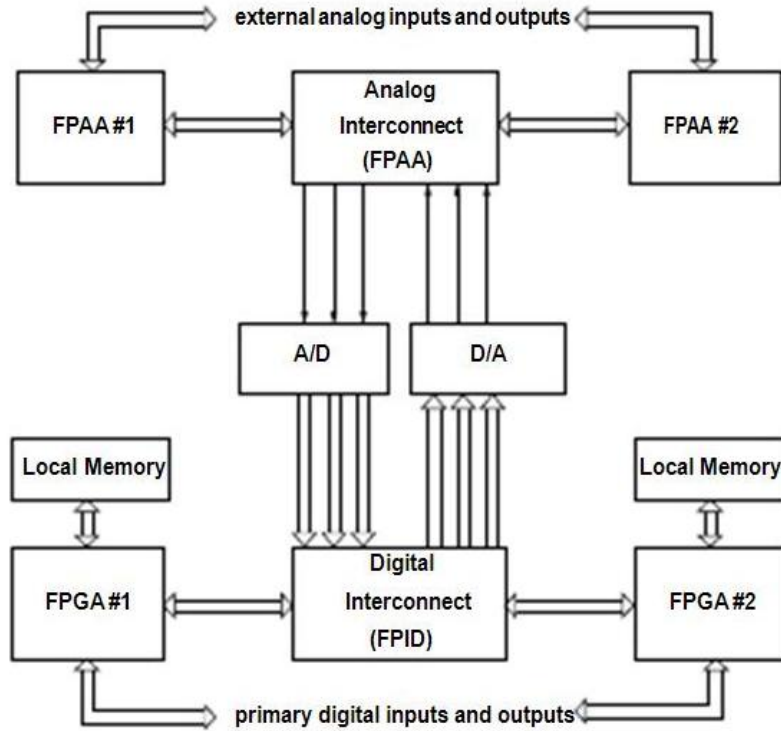


Figure 1. FPAF - PFPA Architecture proposed See fig. 3 to review the FPGA Development Board applied in this experiment...

Nevertheless, figure 4 shows the strategy used to obtain the improved design with the hybrid architecture. The equation described by the Analog designer group was determined to generate the frequency response for the FPGA in terms of the changes in the noise signal.

The adjust loop is realized by the disability of the PIC in the FPAF Board and the signals paths for the FPGA Development Board as well.



Figure 2. Altera Max II Development Board In this board, a EPM1270 FPGA is described the PIC used in the FPAA prototyping board to adapt the frequency response for the Front-End scheme.

Scheduling the firing signals for each SC sub-circuit the adaptive algorithm is obtained.

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Figure 5 is showed to describe the form to pre-programming the internal architecture of the adaptive filter.

Then Figure 6 and 7 show the Bode and Z-states for the first approach and obtaining the primary result for the Front -End in figure 8.

Figure 8 let to compare the simulation result of the actual filter installed in the Front-End of ACORDE-ALICE architecture. The simulator is Modelsim for Quartus II Web Edition. Note the Noise correlated at the signal with at reduction obtained of 10

In this case, Channel 1 is the original Front-End signal and Channel 2 shows the output for the adaptive filter. The noise reduction is about 5% with the architecture proposed.

4 Results

We begin by considering a simple special case. Obviously, every simply simulation demonstrate the possibility to improve the noise reduction in the signal. Clearly, if the design provide the advantages for the mixed-design then some requirements must be satisfy. Because the Clock signal for the FPAA is adjusted at the noise-event, if the change is intermittent to the velocity response for the device then is undesirable, non-suitable and with unstable behavior. Therefore if the architecture is stable then it will be applies for a specific ranges of signal values for event.

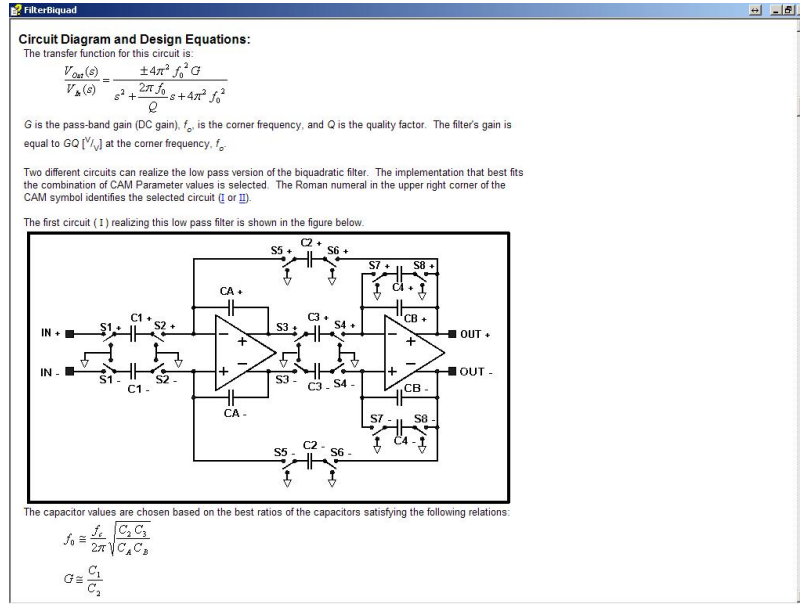


Figure 3. Design scheme based on FPAA Architecture.

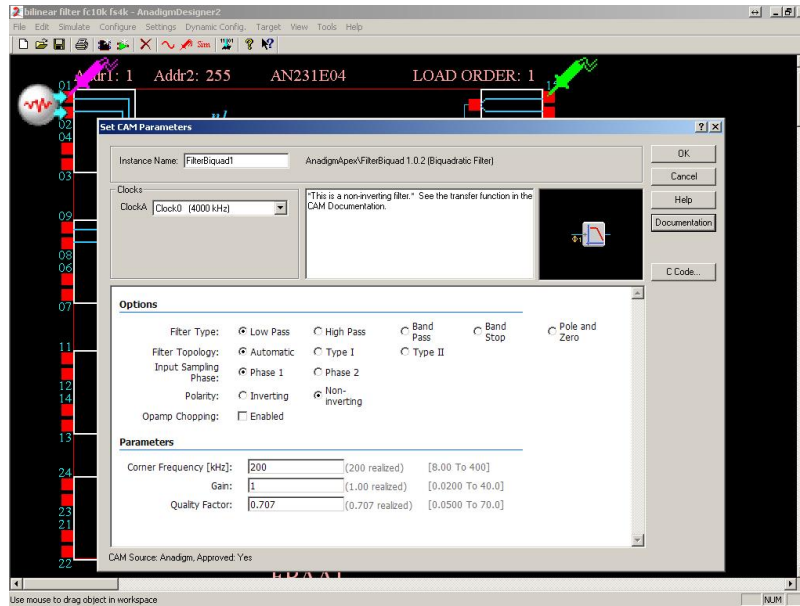


Figure 4. Design platform for FPAA Architecture

4.1 Residual Analysis with Autocorrelation.

In this part a statistical analysis shows how to use autocorrelation with a confidence interval to analyze the residuals of a least-squares fit to noisy data in both two signal i.e. the original front-end filter design (Ch1) and the improved signal measured at the output of the FPGAA adaptive architecture Ch2. Then the residuals are the differences between the fitted model (Ch1) and the data (Ch2).

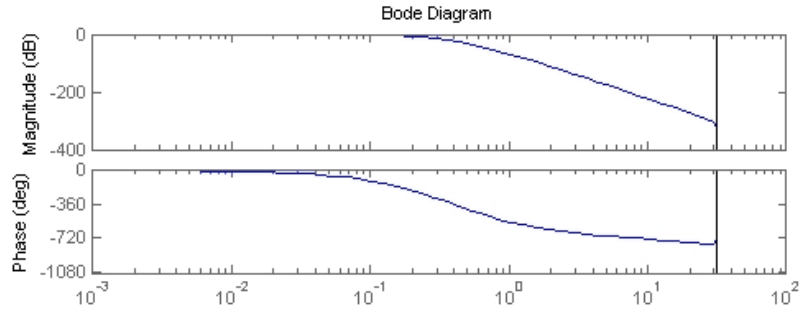


Figure 5. Frequency response

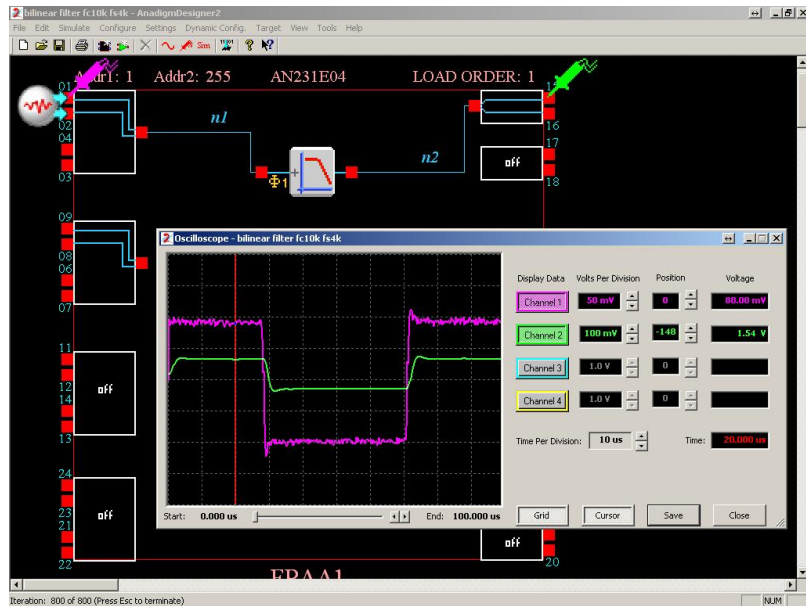


Figure 6. Results using FPAA architecture

Considering the theory proposed in a signal-plus-white noise model, if a good fit for the signal is proposed, the residuals should be white noise.

The additive noise is a sequence of uncorrelated random variables following a $N(0,1)$ distribution. This means that all the random variables have mean zero and unit variance. Set the random number generator to the default settings for reproducible results.

The analysis was export at classical algorithm developed for Matlab because it is an adequate platform for signal analysis considering the toolboc added in its environment.

Using the polyfit command to find the least-squares line for the noisy data it is possible to plot the original data along with the least-squares fit showed in figure .

Findind the residuals, it is necessary to obtain the autocorrelation sequence of the residuals to lag 50. When you inspect the autocorrelation sequence, you want to determine whether or not there is evidence of autocorrelation. In other words, you want to determine whether the sample autocorrelation sequence looks like the autocorrelation sequence of white noise. If the autocorrelation sequence of the residuals looks like the autocorrelation of a white noise process, you are confident that none of the signal has escaped your fit and

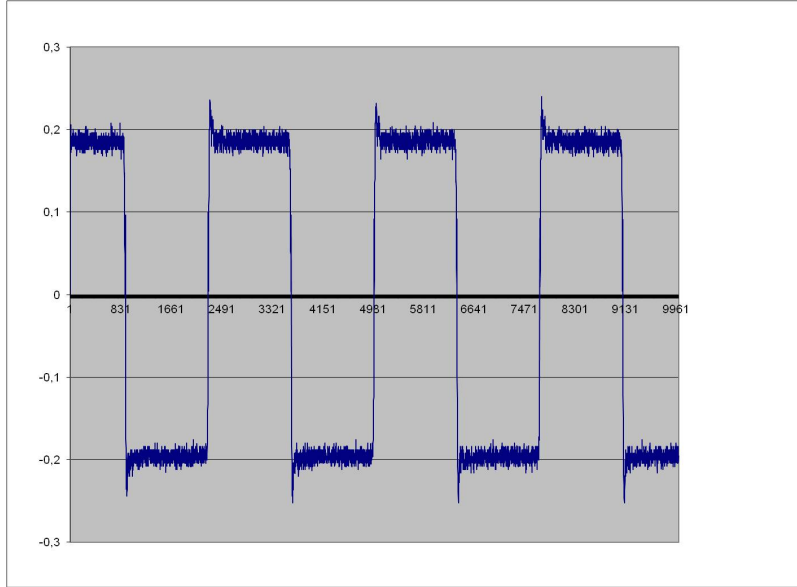


Figure 7. Original ACORDE Front-End signal

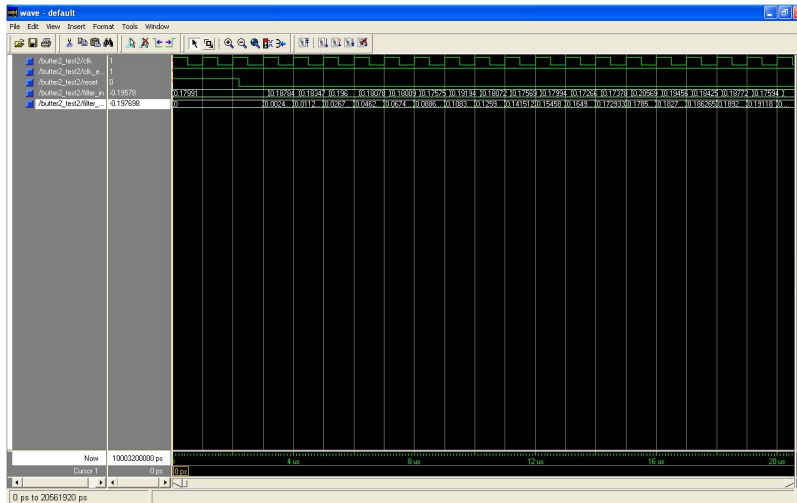


Figure 8. Pulses on Single FPGA architecture

ended up in the residuals. In this analysis, a 99% confidence interval is applied. To construct the confidence interval to know the distribution of the sample autocorrelation values is needed. But also to find the critical values on the appropriate distribution between which lie 0.99 of the probability is defined.

Because the distribution in this case is Gaussian, a complementary inverse error function is required. The matlab command is defined as `erfcinv`. The relationship between this function and the inverse of the Gaussian cumulative distribution function is described on Matlab Help Page.

In figure 12, the complete algorithm is described. The principal steps can be resumed as follows:

1) Fitting the data. 2) Defining the experiment for White noise. 3) Finding the critical value for the 99% confidence interval. 4) Using the critical value to construct the lower and upper confidence bounds. 5)

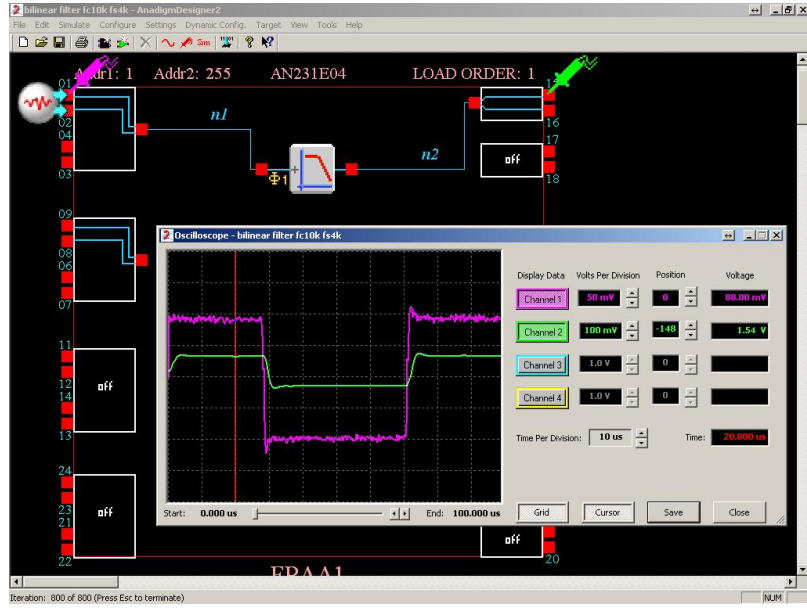


Figure 9. Signal result with new architecture

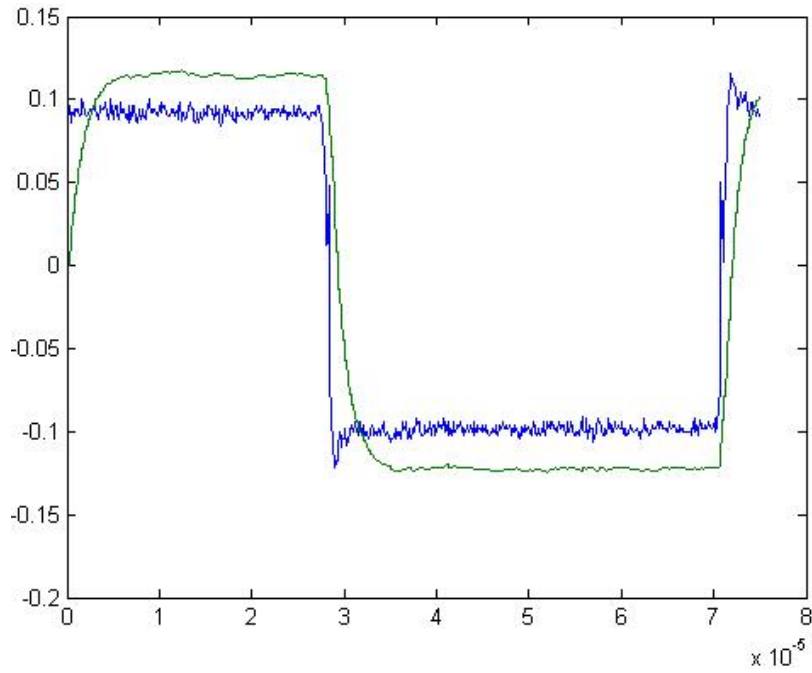


Figure 10. Replace this text with your caption

Plotting the autocorrelation sequence along with the 99% confidence intervals.

Except at zero lag, the sample autocorrelation values lie within the 99% confidence bounds for the autocorrelation of a white noise sequence. At this part of the analysis, it can conclude that the residuals are white noise. More specifically, it cannot reject that the residuals are a realization of a white noise process for

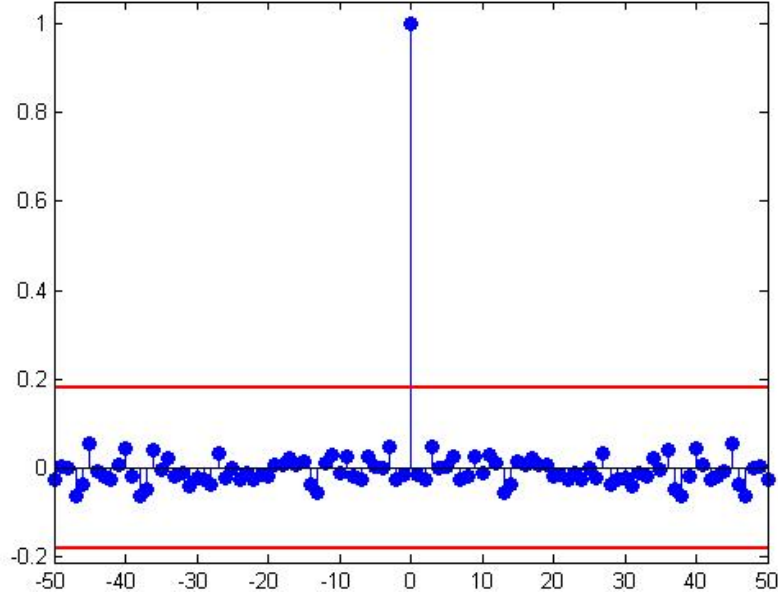


Figure 11. White noise comparing

both signals.

Now, considering that the data are sampled at 100 kHz then the frequency of the experiment can be set for the random number generator to the default settings for reproducible results.

Using the discrete Fourier transform (DFT) to obtain the least-squares, then, the random signal is fitting to both channels 100 kHz. The least-squares estimate of the amplitude is $2 / N$ times the DFT coefficient corresponding to 100 kHz, where N is the length of the signal. In this part, DFT bin 101 corresponds to 100 kHz. Find the residuals and determine the sample autocorrelation sequence to lag 50.

Therefore, plotting the autocorrelation sequence with the 99% confidence intervals. Again, except at zero lag, the sample autocorrelation values lie within the 99% confidence bounds for the autocorrelation of a white noise sequence.

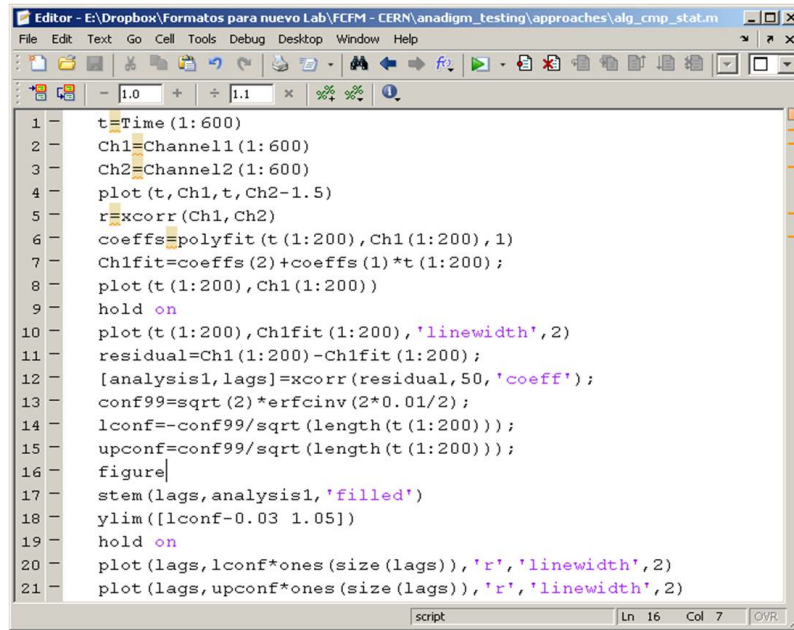
From this, it is concluded that the residuals are "white noise". More specifically, it is not possible to reject that the residuals are a realization of a white noise process.

Finally, add another sine wave with a frequency of 200 Hz and an amplitude of $3/4$. Fit only the sine wave at 100 Hz and find the sample autocorrelation of the residuals.

In this case, the autocorrelation values clearly exceed the 99% confidence bounds for a white noise autocorrelation at many lags. Here you can reject the hypothesis that the residuals are a white noise sequence. The implication is that the model has not accounted for all the signal and therefore the residuals consist of signal plus noise.

5 Conclusions

This work shows the analysis and modeling with a proposed mixed-mode architecture based and FPAA-FPGA architecture which have been applied in the ALICE/ACORDE Front-end platform with adequate result in the noise reduction index. To demonstrate the feasibility of this design, a typical noise analysis is realized using Matlab scheme and the interconnection with the scheme is developed by Integration architecture of both FPAA-FPGA software. Some power and program adjusts are been made to adapt the new approach, at the Front-end system in the actual ALICE/ACORDE experiment tyo increase the performance of the same



```
1 t=Time(1:600)
2 Ch1=Channel1(1:600)
3 Ch2=Channel2(1:600)
4 plot(t,Ch1,t,Ch2-1.5)
5 r=xcorr(Ch1,Ch2)
6 coeffs=polyfit(t(1:200),Ch1(1:200),1)
7 Ch1fit=coeffs(2)+coeffs(1)*t(1:200);
8 plot(t(1:200),Ch1(1:200))
9 hold on
10 plot(t(1:200),Ch1fit(1:200),'linewidth',2)
11 residual=Ch1(1:200)-Ch1fit(1:200);
12 [analysis1,lags]=xcorr(residual,50,'coeff');
13 conf99=sqrt(2)*erfcinv(2*0.01/2);
14 lconf=-conf99/sqrt(length(t(1:200)));
15 upconf=conf99/sqrt(length(t(1:200)));
16 figure
17 stem(lags,analysis1,'filled')
18 ylim([lconf-0.03 1.05])
19 hold on
20 plot(lags,lconf*ones(size(lags)),'r','linewidth',2)
21 plot(lags,upconf*ones(size(lags)),'r','linewidth',2)
```

Figure 12. Matlab Algorithm

one as well. The signal obtained in the final process was a better SNR value in comparison with the previous one.