A Capacitor-Free CMOS Low-Dropout Regulator with Gate-Couple Flipped Voltage Follower for SOC

Yani Li[1], Fuxiang Tong[1], Zuoyi Zhang[1], Zhuo Lv[1], Linkun Zhang[1], and Zhangming Zhu[1]

[1]Xidian University School of Microelectronics

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Abstract

This paper proposes a fully integrated low dropout (LDO) regulator with gate-couple flipped voltage follower(GC-FVF). The proposed GC-FVF addresses the limited output swing issue of conventional PMOS FVF in LDOs while maintaining a low output impedance. Besides, this LDO introduces a cascode compensation loop, which, along with the low output impedance of GC-FVF, pushes the output pole far away from the unity-gain bandwidth under both light and heavy load conditions. Consequently, the LDO becomes a stable two-pole system, supporting a high loop gain of up to 100dB and significantly enhancing the load and line regulation. Key specifications include a preset output voltage of 1.8V, a minimum unregulated input voltage of 2V, a maximum output current of 100mA, a ground current of 32μA, and an active chip area of 260μm×180μm. Notably, this LDO achieves high load regulation of 4.8μV/mA and high line regulation of 13.8μV/V without the need for off-chip capacitors.

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Yani Li, Fuxiang Tong, Zuoyi Zhang, etc. are all with Shaanxi Key Lab of Integrated Circuits and Systems, School of Microelectronics, Xidian University, 2 South Taibai Road, Xi'an, 710071, P. R. China. (E-mail: 21111212988@stu.xidian.edu.cn).

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This paper proposes a fully integrated low dropout (LDO) regulator with gate-couple flipped voltage follower(GC-FVF). The proposed GC-FVF addresses the limited output swing issue of conventional PMOS FVF in LDOs while maintaining a low output impedance. Besides, this LDO introduces a cascode compensation loop, which, along with the low output impedance of GC-FVF, pushes the output pole far away from the unity-gain bandwidth under both light and heavy load conditions. Consequently, the LDO becomes a stable two-pole system, supporting a high loop gain of up to 100dB and significantly enhancing the load and line regulation. Key specifications include a preset output voltage of 1.8V, a minimum unregulated input voltage of 2V, a maximum output current of 100mA, a ground current of 32μA, and an active chip area of 260μm×180μm. Notably, this LDO achieves high load regulation of 4.8μV/mA and high line regulation of 13.8μV/V without the need for off-chip capacitors.

1. Introduction

As an important research field in analog chips, power management is widely used in various electronic products. The low dropout voltage (LDO) regulator is one of the most considerable power management modules, which can provide an adjustable low noise and precise power supply voltage for noise sensitive analog blocks. The characteristics of LDOs make them widely used in highly integrated electronic devices such as mobile phones, pagers, video recorders, laptops. In addition, the improvement of integration level in

portable devices not only requires LDOs to provide high load current, but also requires LDOs to minimize no-load quiescent current to extend battery life [1-2]. In many existing topologies, the LDO based on the fully integrated flipped voltage follower (FVF) is an attractive choice due to its low output impedance, fast transient response, and relatively small area [3-6].

Fig.1(a) shows the conventional CD amplifier structure, which needs a current bias from the positive supply. Fig. 1 (b) shows the conventional PMOS FVF circuit [4]. The gate of M2 is connected to the feedback terminal V_{FB}, forming a local feedback loop, which significantly reduces the output impedance [6]. According to the comparison, it can be found that FVFs can be considered as a variant of a common drain (CD) circuit with local feedback.

One major drawback of the conventional PMOS FVF in Fig.1(a) is the limitation on the minimum and maximum load currents and output voltage [3]. If the load voltage is less than the minimum value, the gate voltage of M2 increases to reduce the overdrive voltage, which pushes M1 out of saturation. That is undesirable for the normal function of LDO. And under high load current, the output dominant pole may approach the internal non-dominant pole, resulting in poor phase margin. Besides, due to the low loop gain of FVF, this type of LDO has a substandard load regulation. The poor load regulation is also due to the lack of tight coupling between V_{OUT} and V_{REF}.

Fig. 1. (a). CD amplifier, (b) PMOS FVF structure, (c) Proposed GC-FVF structure

The output voltage range of the PMOS FVF circuit is given by the following equations:

where V_{SG} and $V_{SD,\ sat}$represent the source-to-gate and overdrive voltages, respectively.

Fig. 2. The single transistor controlled FVF LDO in [5]

The single transistor controlled LDO in [5] based on PMOS FVF is shown in Fig. 2, which consists of an error amplifier (EA), a V_{SET} generation stage, and an FVF output stage. The voltage V_{MIR} is adjusted by EA to set V_{MIR} equal to V_{REF}. V_{SET}generation stage establishes a correlation between $V_{MIR}$and V_{OUT}. The transistor M3 connected to V_{SET} through a diode is kept one V_{SG}below V_{MIR}. It can be observed that $V_{MIR}$and V_{OUT} are equal.

Fig. 1 (c) illustrates the proposed GC-FVF structure, separating the drain of M1 from the gate of M2 by using a coupling capacitor C1, which maintain the advantage of small impedance without shrinking the output swing.

The proposed GC-FVF structure solves the voltage swing problem of a PMOS FVF as the output stage, while retaining the low output impedance characteristic of PMOS FVFs.

The organization of this article is as follows: Section II describes the implementation details of the proposed GC-FVF structure. Section III analyzes the overall loop of LDO with the proposed GC-FVF as the output stage. Section IV presents simulation results and compares them with other literature. Section V discusses the conclusions.

2. Proposed Gate-Couple Flipped Voltage Follower

As shown in Fig. 3(a), the drain of M1 is separated from the source of MP by using a capacitor C1. MP is the power transistor for this LDO. The gate of M1 has been changed to connect a bias voltage instead of a reference voltage in FVFs. The parasitic capacitors $C_{GS,\ pass}$, and $C_{GD,\ pass}$ associated with MP are large and usually comparable to the output capacitor. At low frequency, as illustrated in Fig. 3(b), C1 is considered to be open. However, at high frequency, C1 is considered to be a relatively opening path, at which point the FVF structure works, as illustrated in Fig. 3(c).

Fig. 3. (a). GC-FVF structure, (b) Situation at low frequency, (c) Situation at high frequency

Two different operating modes between high and low frequency keep the output impedance change within a moderate range. And the isolation of the capacitor can eliminate the impact of the DC voltage of MP's

gate on the DC operating point of M1.

The proposed GC-FVF structure maintains low output impedance in unity-gain bandwidth while allowing the swing of the output voltage V_{OUT} to be independent of the load current. According to the calculation of *vx* and *ix* in Fig. 3(a), the small signal output impedance under typical application conditions of the proposed GC-FVF structure can be calculated as follows:

where $C_{tot} = C_1 + C_{GD} + C_{GS}$. Parameters g_{m1} and $g_m$represent the transconductance of M1 and MP.

In the case of an FVF application where g_{m1} andg_{mp} are approximately equal. And$C_1 >> C_{GD}$, C_{GS}, poles $\omega_{\Pi 1}$ and$\omega_{\Pi 2}$ are given by

The molecule of the impedance transfer function represents the existence of a zero in the left-half-plane (LHP), which is given by

The impedance comparison diagram of the conventional PMOS, PMOS FVF, and Gate-couple FVF is illustrated in Fig. 4. As shown, the appearance of the zero point stabilizes the impedance in the mid frequency range, while at high frequency, the impedance is similar to that of FVFs.

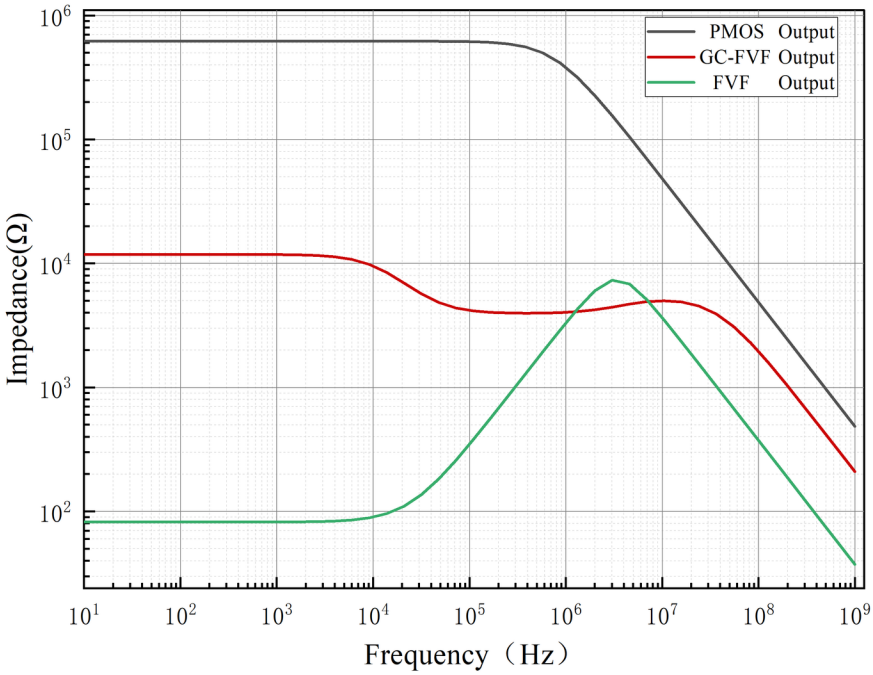

Fig. 4. Output impedance characteristic of PMOS, GC-FVF and FVF topologies.

For FVFs, at low frequency, the low impedance affects its loop gain, and at high frequency, the impedance may increase, further affecting its loop stability. The proposed GC-FVF has a moderate output impedance at low frequency that is between the PMOS FVF and the conventional PMOS structures, which avoids its DC gain from being small. At high frequency, C1 is considered to be a relatively opening path, so the PMOS FVF works, reducing the variation of its impedance with frequency. Intuitively, the GC-FVF structure utilizes the impedance characteristic of the gate-couple capacitor, which can block the DC voltage while allowing the PMOS FVF structure to work at small-signal state without affecting the output voltage swing of the LDO.

Fig. 5 shows the output impedance with frequency of the LDO with GC-FVF structure. g_{m1} is a constant, whileg_{mp} is determined by the load current. As the load current I_{load} varies from a light load of 10μA to a

heavy load of 100mA, the transconductance of the pass transistor increases, resulting in the decrease of the output impedance. Importantly, there will be a large peak at 15MHz under light loads, while such problems will not occur under heavy loads.

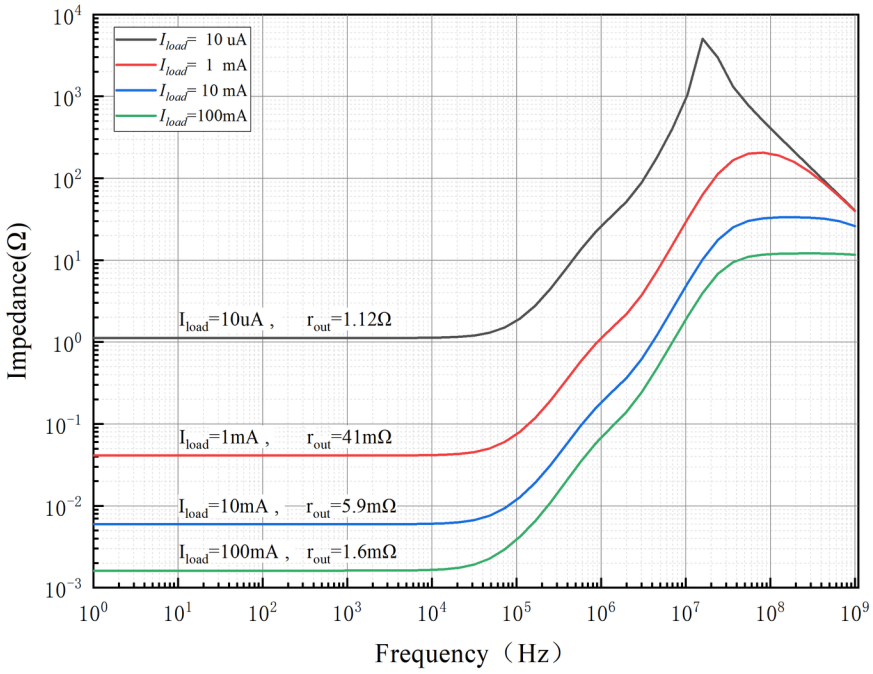

Fig. 5. Output impedance characteristic of the proposed GC-FVF LDO.

3. Circuit implementation

Fig. 6 shows the overall structure of the proposed GC-FVF LDO. The error amplifier (EA) consists of a single-stage folded cascode structure, with the PMOS M1 and M2 being the input stage. According to previous discussions, the output swing of FVF structures such as STC-LDO in [5] is severely limited, and a NMOS is consequently required as the input pair. M9 is a PMOS buffer with a small output impedance, which pushes the poles at N1 to a high frequency. The common source gain stage is achieved through the power PMOS MP and constitutes the second gain stage in the LDO to drive the on-chip output capacitor CL. On-chip resistors R1 and R2 form a negative feedback by sampling the output voltage and feeding it back to the noninverting input terminal of the EA. Therefore, the obtained LDO structure can be considered as a two-stage amplifier.

Fig. 6 Structure of the proposed LDO with Gate-Couple FVF scheme

3.1. Frequency compensation method

The proposed LDO is stabilized by a cascode miller frequency compensation, which is a kind of pole-splitting compensation method. The compensation capacitor Cc provides a low-frequency pole for the two-stage amplifier to achieve stability over the entire range of load current. In this two-stage amplifier design, the use of a cascode miller frequency compensation scheme enables the amplifier to achieve a wider unity-gain frequency and higher stability by removing the right half plane zero point, as well as enhances the PSRR [2].

In addition, and more importantly, this compensation design is used to split the pole at the LDO output, allowing the LDO to achieve stability throughout the entire load current range by using only small compensation capacitors. Fig. 6 shows the cascode Miller frequency compensation in the proposed LDO, implemented by Cc and transistor M3.

3.2. Proposed GC-FVF output stage

The proposed GC-FVF structure consists of M5, C1 and MP in Figure 6. M6 and M24 provide the gate bias voltage and drain bias current for M5 respectively, and the GC capacitor C1 is coupled from the drain of M5 to the gate of the transistor MP.

The output voltage range of this LDO is given by

where V_{GS} and $V_{DS,\ sat}$represent the gate-to-source and overdrive voltages, respectively.

The FVF output stage can be considered as a fast loop, which has been analyzed in the previous section that can provide output impedance attenuation without affecting the output voltage swing or load current range. It can be inferred that the attenuated output impedance and the small on-chip load capacitance keep the output pole constantly away from the unit gain bandwidth. It is worth mentioning that this fast loop has a role in transient response.

3.3. Stability Analysis

It is important to analyze the stability of the proposed LDO using the loop gain transfer function. Figure 7 is the small signal block diagram of the circuit in Fig. 6, used to analyze the open-loop transfer function. The g_{m1} , g_{m3} ,g_{m5} , and g_{mp} in Fig. 6 represent the transconductance of the input differential stage M1/M2, current buffer stage M3, gate-couple feedback input stage M5, and power transistor MP, respectively. In addition, β =R2/(R1+R2) is the feedback coefficient. The output of the source follower N1 is a low impedance node, so the parasitic capacitance here is ignored in the analysis. The loop gain transfer function is given by

Based on the above settings, the zero can be ignored and the poles of the proposed GC-FVF LDO are given by

Fig. 7 Small-signal block diagram of the proposed LDO with current-buffer compensation scheme.

The following points are referred to:

1. The GC-FVF structure makes little variation of the output impedance within the unity-gain bandwidth.
2. The minimum current and gm of MP is limited by the DC operating points of M5 and M6.
3. No large off-chip load capacitance.

Therefore, under both light and heavy loads, the value of$R_{out_eq}C_L$ is a relatively small, so the circuit can be regarded as a stable two-pole amplifier system composed of $\omega_{\Pi 1}$ and $\omega_{\Pi 2}$. Figure 8 shows the bode plot of the proposed GC-FVF LDO. It can be seen that under heavy load, due to the decrease in gain, the main pole$\omega_{\Pi 1}$ is extrapolated, but it is still relatively far away from the non-dominant pole. Figure 8 shows that the phase margin remains almost unchanged under light and heavy loads.

Fig.8 Simulated loop-gain transfer function of the proposed GC-FVF LDO.

4. Simulation result

To test and verify the proposed GC-FVF LDO, this chip is shown in Fig. 6 which is manufactured in a 0.18μm standard 5V CMOS process. Fig. 9 shows the layout of the proposed LDO, with an effective area of 260μm×180μm. The regulator is designed to provide a load current of 0-100 mA with an output voltage of 1.8 V from a 2 to 5V supply. The dropout voltage is about 200 mV at the maximum I_{load} .

Fig. 9 Layout of the proposed GC-FVF LDO

The line regulation and load regulation

Benefiting from a stable two-pole system, the loop gain of the proposed LDO can exceed up to 100dB. And the load and line regulation are given by

Fig. 10 shows the load transient response of the GC-FVF LDO at a Vin of 3.3V. Fig. 11 shows the line regulation from 0mA to 100mA at Vin=2V, 2.5V and 3.3V. The measured line and load regulations are 13.8

μV/V and 4.8 μV/mA, respectively.

Fig. 10. Simulated load transient response

Fig. 11. Simulated load regulation

Transient response

Compared with the example in [12] without off-chip capacitors, the proposed LDO has an improved transient response. Fig. 11 depicts the measured transient response with an on-chip load block whose current changes from 0mA to 10mA, 50mA and 100mA within 1μs. Under a large load step change from 0mA to100mA, the transient overshoot and undershoot are 367mV and 202 mV. The proposed GC-FVF loop improves the transient response of the LDO without off-chip capacitors, and the good transient stability of the output voltage further proves the large phase margin achieved in the proposed LDO.

To compare this work with other LDOs in the literature, widely used figure-of-merit (FOM) are adopted from [11]. The FOM is defined as

where T_R is the transient response time,I_Q is total quiescent current andI_{MAX} is the maximum load current. This indicates that LDOs with better power consumption and transient performance have lower FOM.

Table 1. Performance comparison with related works. (*Experimental Results)

	This Work	ICET 2023[13]	TCAS-II 2023[8]	MWSCAS 2017[7]	TCAS-I 2016[9]	JSSC 2012 [10]
Process[nm]	**180**	180	28	180	500	45
Max load current[mA]	**100**	50	20	10	150	42
I_Q(μA)	**32**	91.6	135	53-93	40	12000
Input voltage [V]	**2-5**	1.4-1.8	0.96	1.5	2.3-5.5	1.2-1.6
Output voltage [V]	**1.8**	1.2	0.9	/	1.2-5.4	0.9-1.1
Off-chip capacitor	**no**	no	no	yes	yes	yes
Chip area[mm^2]	**0.047**	0.0136	0.044	/	0.28	0.003
Load regulation (μV/mA)	**4.8**	16	240	31	0.24*	83*
Line regulation (μV/V)	**13.8**	12.5	/	/	0.42*	27000*
FOM(pS)	**26**	/	/	3.9	/	62.4

Table. 1 shows that the proposed LDO has a low quiescent current of 32μA, resulting in better FOM compared to the LDO in [10] without off-chip capacitors. With a low output impedance within the unity-gain bandwidth, the proposed LDO still has a wide input voltage swing, while the input voltage of the conventional FVF LDO in [5] must be about one V_{TH} larger than V_{OUT}. In addition, benefiting from high loop gain, this LDO has better load regulation of 4.8μV/mA and line regulation of 13.8μV/V compared to those in [7-8] while maintain a small area about 0.047 mm^2 and low power dissipation of 32μA.

5. Conclusion

This work proposes an LDO based on GC-FVF structure. The proposed GC-FVF structure solves the swing problem of PMOS FVFs as the output stage, while retaining the low output impedance characteristic. This, combined with cascode Miller frequency compensation, can generate two stable poles inside the LDO, while the output pole is pushed far away from the unity-gain frequency.

The simulation results show that the GC-FVF LDO has improved transient response compared to other LDOs without off-chip capacitor. And this chip has a wide input and output range, high load and linear regulation, low quiescent dissipation, and high load current.

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