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MEDSA: A Memristive-passive Delta-Sigma ADC Circuit for Detecting Neural Signals

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***Abstract*—In this study, we present an analog-to-digital converter (ADC) optimized for implantable neural interfaces. The proposed ADC integrates a series of memristors in both the input and feedback Digital-to-Analog Converter (DAC), significantly boosting the input impedance and making it suitable for neural interfaces. A defining feature of the ADC is the ability of the memristor resistance to adapt to various conditions such as large DC offset, motion, and stimulation artifacts. The model was simulated using 65nm MOSFET technology along with a physical memristor model, yielding an impressive signal-to-noise-and-distortion ratio (SNDR) of 62.7dB and a substantial Nyquist sampling rate of 50kHz. Power consumption is remarkably low, with less than nW for integrators, 5µW for the comparator, and 0.45 μW for the feedback DAC - a key requirement for neural interfaces implanted in the brain. The ADC demonstrates strong resilience against component mismatch, maintaining circuit stability even in variable conditions. Through its ability to adjust input resistance, the ADC can enhance its SNDR. This adaptive and robust ADC design shows promising potential for implantable neural interface applications.**

***Index Terms*—$\Delta\Sigma$ ADC, Memristor, Passive integrator, Saturation protection**

I. Introduction

Implantable neural interfaces represent a significant leap forward in tackling a range of neurological disorders. Fig. 1 illustrates the primary components of a typical neural interface. The interface functions by recording data from the neural side, subsequently converting this analog data into a digital format [1], [2]. This digitized data is then relayed to a wearable or handheld device for comprehensive analysis. If an abnormal signal is detected, the wearable or handheld device is engineered to send a corrective command to the implant, which activates the stimulator to suppress the irregular signal. A pivotal component enabling these functionalities is the analog-to-digital converter (ADC), which significantly impacts the quality of the recorded signal and thereby, the accuracy of abnormal signal detection.

With the necessity for high-fidelity neural signal recordings, which are characteristically low in amplitude and bandwidth, delta-sigma ADCs emerge as the optimal choice for digitization. Their intrinsic loop filter is capable of mitigating low-frequency quantization noise, resulting in a superior signal-to-quantization noise ratio, even with a one-level quantizer. Nevertheless, conventional delta-sigma ADCs are not without limitations, rendering their integration into high channel count neural interfaces a complex task. These constraints also pose challenges for their direct application in neural interface scenarios.

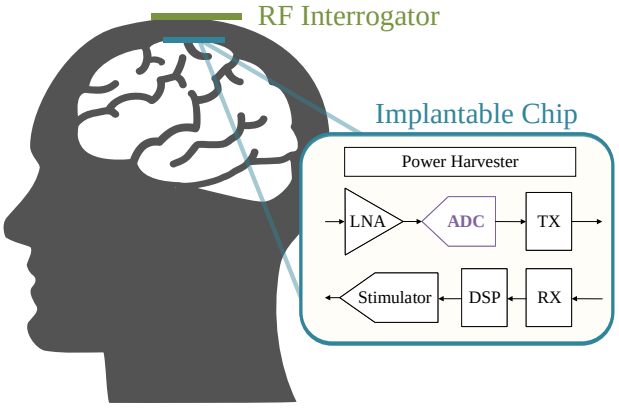

Fig. 1. The architecture of implantable neural interface, which is mainly composed of RF interrogator and implantable chip.

To overcome the challenges associated with traditional delta-sigma ADCs, this paper proposes a memristor-based delta-sigma ADC that addresses the aforementioned limitations. The organization of this paper is as follows: Section II provides a review of the state-of-the-art delta-sigma ADCs used in neural interface analog front-end designs and discusses their strengths and weaknesses. In Section III, we introduce the operational mechanisms of the proposed memristor-based delta-sigma ADC, followed by an in-depth examination of the circuit implementation. Finally, the operational procedure is detailed and supported by an evaluation of the simulation data.

II. The State of Art Neural ADC

Figure 2(a) illustrates a conventional 1st-order delta-sigma ADC, primarily using an integrator to suppress low-frequency quantization noise. Despite its functionality, this design encounters several substantial limitations. Primarily, the requirement for an integrator results in considerable power consumption, constraining its applicability within high channel count implantable devices. Moreover, the integrator introduces low-frequency flicker noise [4], thereby deteriorating the quality of the recorded signal. This is particularly problematic in the context of neural signal detection, characterized by their low-amplitude and low-frequency nature [5], [6]. Consequently, achieving an optimal trade-off between power, area, accuracy, and noise reduction in such power-hungry active circuits

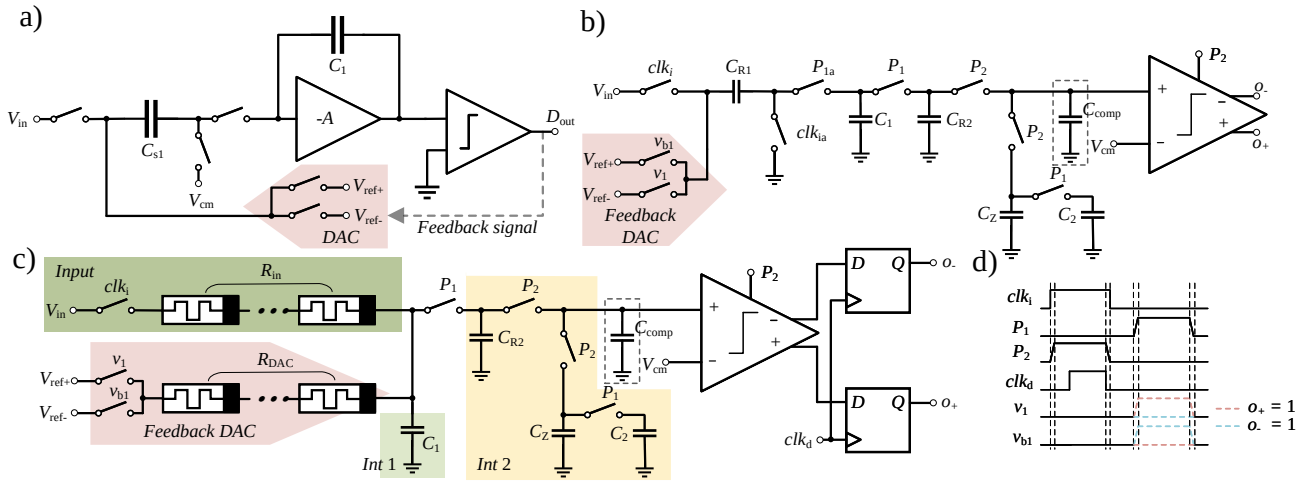

Fig. 2. (a) A general structure of conventional 1^{st} order $\Delta\Sigma$ ADC, with switch capacitor OTA and a DAC, which gives feedback to the integrator. (b) A general structure of conventional passive 2^{nd} order $\Delta\Sigma$ ADC realized by two lossy integrators C_1 and C_2 [3]. (c) Proposed resistive passive 2^{nd} order $\Delta\Sigma$ ADC realized by memristor input and feedback DAC. (d) The timing diagram of the proposed ADC is shown in (c).

proves to be challenging. Secondly, the innate sample-and-hold circuit embedded within the design diminishes the input impedance, which might lead to a potential compromise in signal quality. Further complications arise due to the integrator's susceptibility to saturation, attributable to the DC offset linked with electrode-induced stimulation and motion artifacts.

The work presented in [7], [8] implements an additional delta modulation on the traditional delta-sigma ADC. A delta modulator is positioned at one terminal of the sampling capacitor, generating a voltage nearly analogous to the input signal sampled in the previous clock phase, while the input signal is concurrently sampled at the other terminal. This configuration ensures that the charge transferred to the integrator is proportional to the difference between consecutive samples rather than the input signal itself. This approach mitigates the risk of integrator saturation due to DC offset and enhances the DC input impedance by reducing the charge entering the integrator and the sampling capacitor. However, the full functionality of this method still depends on the use of a power-consuming integrator.

The studies by [9], [10] incorporate a passive second-order loop filter in the delta-sigma ADC, mitigating the limitations of the power-intensive integrator. As illustrated in Fig. 2(b), capacitors C_1 and C_2 serve as lossy integrators, replacing the active amplifiers, significantly reducing both power consumption and low-frequency noise. The system's stability is reinforced by an additional pole added by the capacitor C_z. The capacitor C_{R1} samples the input and feedback, channeling them to the first integrator, while C_{R2} samples the output of the first integrator, feeding it to the second. The comparator's input impedance is represented by C_{comp}. Nevertheless, this strategy necessitates additional circuitry to increase the input impedance and manage complications from the DC offset and stimulation artifacts, complicating the system design.

In light of the aforementioned challenges, this paper introduces another design method for a delta-sigma ADC. The design incorporates a memristor-based passive loop filter, which adeptly mitigates the issues of DC offset and stimulation artifacts. Concurrently, it enhances the input impedance, eliminating the need for a power-consuming integrator.

III. Proposed Neural ADC

The proposed resistive passive second-order $\Delta\Sigma$ ADC is depicted in Fig. 2(c). In this architecture, the conventional input sampling capacitor C_{R1} in Fig. 2(b) is replaced with the resistive input (in dark green) and the feedback DAC (in pink). These replacements are realized through a series connection of multiple memristors to establish an increased input resistance R_{in} and feedback DAC resistance R_{DAC}. While the second integrator remains unmodified, the resistive integrator, comprised of R_{in} and C_1, exhibits an approximate transfer function as follows:

$$H_1(z) = \frac{V_{out}(z)}{V_{in}(z)} = \frac{1}{f_S C_1 R_{in}} \frac{1}{1-(1-\frac{1}{f_S C_1 R_{in}})z^{-1}} \quad (1)$$

When $f_S C_1 R_{in}$ is sufficiently large, and ΔV_{C1} is significantly smaller than ΔV_{in}, function (1) turns to,

$$H_1(z) \approx \frac{1}{f_S C_1 R_{in}} \frac{1}{1-z^{-1}} \quad (2)$$

A latched comparator with inverters at the differential outputs is utilized to boost the comparator's gain.

Fig. 2(d) presents a timing diagram showcasing the primary operational stages of the proposed ADC. The operation begins with the closure of clk_i, enabling the integration of the input signal on C_1 through R_{in}. Subsequently, closing P_1 triggers the transfer of a minute portion of the charge from C_1 to C_{R2}, enabling C_{R2} to sample C_1's voltage. When P_2 is closed, the charge on C_{R2} is distributed to both C_z and C_{comp}, and the comparator concurrently evaluates its input against the reference voltage. Once the comparator's outputs stabilize, clk_d ascends, capturing and holding the output result

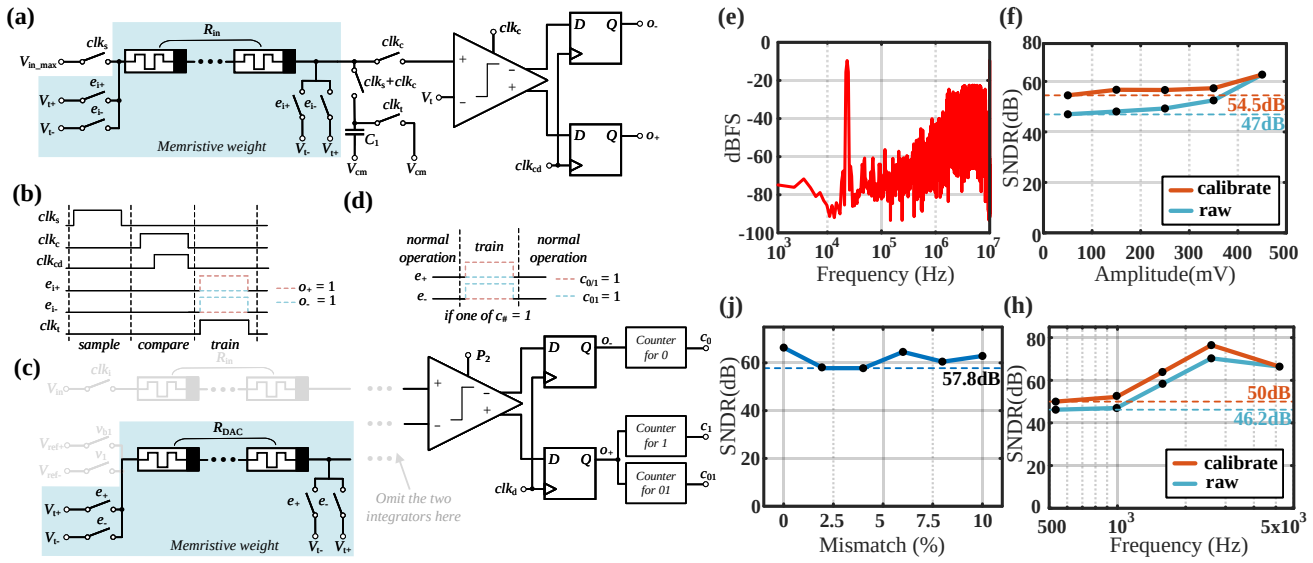

Fig. 3. (a) Calibration circuit for the input memristor series in the proposed ADC. The second integrator in Fig. 1(c) will stop working during this calibration and is omitted in this graph. (b) The timing diagram for the calibration circuit in (a). (c) Calibration circuit for the feedback DAC memristor series in the proposed ADC. The graph omits circuits of two integrators. The circuit will work as normal when feedback DAC memristors are not calibrated. (d) The timing diagram for the calibration circuit in (c). (e) The output spectrum of the proposed ADC under 23kHz input. The rest of the figures are (f) Amplitude sweep, (j) Mismatch test, and (h) Frequency sweep of the proposed ADC

for feedback. Depending on the digital result, either V_1 or V_{b1} of the feedback DAC is closed, prompting the addition or removal of Δq from C_1 via R_{DAC}. The negative feedback maintains V_{c1} relatively stable around V_{cm}.

This approach offers two primary benefits: (1) it substantially increases the input impedance by utilizing a series of memristors within both the input and feedback DAC, thereby ensuring the compatibility of the input impedance with implantable neural interfaces. (2) It enables the memristor resistance to adapt to a variety of circumstances, including electrode DC offsets, motion, and stimulation artifacts. This adjustability, to be discussed in further detail in Section IV, significantly bolsters the robustness of the ADC, enhancing its suitability for implantable neural interface applications.

IV. Adaptation to Neural Signals with Varied Amplitude and Frequency Interferences

In this section, we delineate the methodology implemented for training the memristors embedded within our proposed system. This technique enables the memristors to adapt responsively to neural signals, which often bear interference characterized by an assortment of amplitudes and frequencies. Examples of such interference include electrode DC offsets, manifesting as high-amplitude signals at a zero frequency, and motion or stimulation artifacts, which typically present high-amplitude signals at elevated frequencies.

A. Memristive training

The memristor, a non-volatile passive device, features tunable resistance controlled by its state variable [11]. Its resistance only changes when the applied voltage exceeds V_{on} or drops below V_{off}; otherwise, it remains constant.

Fig. 3(a) (highlighted in blue) illustrates the trainable memristor weight used in the circuit [12][13]. Under regular ADC operation where the memristor's resistance is read through current flow by, switches $e_{i\pm}$ are kept open, thus maintaining the memristor's resistance. During the writing phase, the remaining circuit components are inactive while either e_{i+} or e_{i-} is closed for a defined duration. This action applies a high (or high reverse) voltage that exceeds one of the memristor's threshold voltages across the series of memristors, thereby inducing an increase (or decrease) in the state variable and incrementally adjusting their aggregate resistance. By managing the control signal $e_{i\pm}$ appropriately, the overall resistance of the memristor series can be meticulously trained to the desired value, enabling the ADC to enhance the signal-to-noise-and-distortion ratio (SNDR) under specific operational conditions.

B. Input amplitude adaption

The proposed passive second-order $\Delta\Sigma$ ADC is a feedback system, characterized by a specific transfer function as follows [3].

$$Y(z) \approx X(z) + \frac{E_Q}{GH(z)} + \frac{E_{comp}}{H(z)} \tag{3}$$

where $X(z)$ represents the analog input, $Y(z)$ is the digital output, E_Q denotes the quantization noise, E_{comp} is the comparator thermal noise, G signifies the comparator's gain, and $H(z)$ is the loop filter's transfer function. As the amplitude of the input signal $X(z)$ decreases while the quantization noise stays constant, the ADC's SNDR correspondingly declines. To counterbalance this amplitude decrease, R_{in} is adjusted downwards to a certain extent. This calibration ensures that the charge introduced into C_1 during the sampling stage is maintained at a comparable level, thereby preserving SNDR.

TABLE I
CIRCUIT PARAMETER

Circuit part	Type	Parameter	Value
ADC	Transistor tech		65nm
	Power source	VDD	2.5V
	Sampling frequency	f_s	10MHz
	Bandwidth	f_{BW}	50kHz
	Total Power	P_{total}	$5.45\mu W$
	Input impedance		13MΩ
	OSR	$f_{in} = 23$kHz	200
		$f_{in} \leq 5$kHz	1000
	Capactiors	C_1/C_2	3pF/0.46pF
$R_{in}\&R_{DAC}$	Memristor[14]	$V_{on/off}$	0.3/-0.4V
		$R_{on/off}$	2k/100kΩ
		$k_{on/off}$	$-4.8/2.8mm/s$
		$\alpha_{on/off}$	3/1
	Calibration voltage	V_+/V_-	3.3V/0V
	Precision		6 bits
Comparator	Source voltage	VDD	2.5V
	Power	P_{comp}	$5\mu W$

The calibration circuit is depicted in Fig. 3(a), with the corresponding timing diagram of one training period shown in Fig. 3(b). During this calibration phase, the second integrator is deactivated. Similar to the regular operation phase, the initial sampling stage allows the input current through R_{in} to charge C_1 for $0.5T_s$. Subsequently, the voltage across C_1, denoted as V_{c1}, is compared with a threshold voltage V_t to ascertain if C_1 is charged more or less by the input. Based on this comparison, if V_{c1} is larger than V_t, R_{in} is increased by a unit step via the appropriate feedback e signal; conversely, if V_{c1} is smaller than V_t, R_{in} is reduced by a unit step. Calibration is completed once the comparator output, o_+, yields distinct values between two consecutive training periods, indicating that the desired R_{in} has been achieved.

C. Input frequency adaption

When the input signal's frequency is reduced, V_{in} will be closed to V_{cm} longer than the higher frequency. The ADC digital output thus needs more 0, 1 alternation to approximate these input values. Additionally, when V_{in} is closed to V_{cm}, the input current,

$$I_{in} \approx \frac{V_{in} - V_{C1}}{R_{in}} \tag{4}$$

will be low for a longer time for low-frequency input. Thus, to incentive the alternation of digital output and enlarge the difference between V_{in} and V_{cm}, we calibrate the R_{DAC} to low resistance to push more feedback charge to C_1 each cycle. This will make the V_{C1} varied large between cycles.

Fig. 3(c)&(d) shows the circuits to calibrate the R_{DAC} and the timing diagram of the circuit. The two integrators are omitted from the graph by ellipses. Three counters that count 0, 1, and 0/1 alternations are added at last to provide calibration feedback signals to memristive weight. The circuit during this calibration will continue to normally work until one of the three counter's values exceeds its threshold ($c_\# = 1$) and be interrupted for calibration. When c_0 or c_1 is raised, the corresponding e signal calibrates the R_{DAC} to 1 unit down to increase I_{DAC} for more alternation. And vice versa when $c_{01} = 1$. After the calibration, the circuit will return to the usual quantization until the next $c_\# = 1$.

TABLE II
COMPARISON WITH PASSIVE 2^{nd} ORDER $\Delta\Sigma$ ADC

	This work	[10]	[15]	[16]	[17]	[3]
Input Method	Res	Cap	Cap	Res	Cap	Cap
CMOS Node (nm)	65	130	65	130	130	1200
$f_s(Hz)$	10M	2M	256k	2M	-	10M
Power (μW)	5.45	0.14	0.18	0.47	1275	250
Bandwidth (Hz)	50kHz	10k	3k	500	100k	20k
ENOB(bits)	10.1	8	9.6	11.5	12	10.8
$FoM_w(fJ/conv)$	48.87	27	36.7	162	1550	3400
Calibration?	Yes	No	No	No	No	No

V. EVALUATION

Utilizing 65nm MOSFET technology and the VTEAM memristor model [14], [18], the proposed ADC design minimizes power consumption, critical for implantable neural interfaces. Detailed design features are presented in Table I, and the comparison with existing ADC is shown in Table II. Power consumption is nearly negligible for the two passive integrators, with the comparator and feedback DAC consuming approximately 5.45 μW in total.

The following performance results are evaluated after section IV.B and then IV.C calibration process. With a Nyquist bandwidth of up to 50kHz, the proposed ADC achieves an SNDR of 62.7dB when processing a 23kHz input signal, as illustrated in Fig. 3(e). The ADC's versatility is highlighted when addressing diverse neural signal amplitudes - it enhances the minimum SNDR from 47dB to 54.5dB following R_{in} calibration, as demonstrated in Fig. 3(f).

The proposed ADC design exhibits significant resilience to mismatches. By calibrating both R_{in} and R_{DAC}, potential instability induced by capacitor mismatches in the lossy integrator is effectively mitigated. This robustness is demonstrated via a mismatch sweep at an input frequency of 5kHz, as shown in Fig. 3(j).

The frequency response simulation, shown in Fig. 3(h), reveals stability across frequencies and an improved SNDR up to 76.2dB post R_{DAC} calibration, considering the primary neural signal distribution falls below 5kHz.

VI. CONCLUSION

In conclusion, this paper introduced an ADC design that offers a dual advantage of enhanced impedance and adjustable resistance to accommodate varying interference amplitude and frequencies, such as electrode DC offsets and motion or stimulation artifacts. This adaptability significantly strengthens the ADC's performance for implantable neural interfaces.

Moreover, the ADC's effective use of passive elements minimized power consumption, a critical aspect for implantable neural interfaces. The ADC showed a robust response across the broad range of potential amplitudes in neural signals.

In light of the results, the proposed ADC design shows significant promise for use in implantable neural interfaces,

given its high input impedance, adaptive resistance, and energy efficiency. Future work will explore more advanced calibration techniques to optimize the performance of this design further.

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