Realization of combinational logic circuit based on three terminal memristor

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Abstract

A three-terminal memristor model is developed in order to improve the anti-interference performance of the memristor and address the issue that the resistance value of the conventional two-terminal memristor is readily impacted by voltage. In order to simulate and validate the function of the three-terminal memristor, the logic circuit and multiplication circuit are developed using this model in this work using the cadence ic617 program. According to the findings, the three-terminal memristor multiplication circuit uses less energy than the typical conventional multiplier circuit, consuming only 0.335 uW. The memristor offers the benefits of low power consumption, compact size, and great integratability as a nanoscale device.

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