A Wide-Dynamic-Range PFM-based Digital Pixel Sensor with Dynamically Biased Multiple Integration

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***Abstract*—In this paper, a 500×500 digital pixel sensor (DPS) based on pulse frequency modulation (PFM) is proposed with dynamically biased multiple integration. By sequentially compressing the photo-response curve and dynamically adjusting the bias current, the dynamically biased multiple integration simultaneously improves the dynamic range and the power efficiency of the proposed DPS. To minimize the non-uniformity of the proposed DPS, a modified charge reset circuit is also employed. The proposed DPS is implemented in a 110-nm CMOS process. Post-layout simulation results show that the deviation of photo-response sensitivity and the overall non-uniformity of the proposed DPS are less than ±2% and 1.5%, respectively. The proposed DPS achieves a dynamic range of 120.5 dB with a frame rate of 250 fps and a pixel pitch of 21 μm. Each pixel of the proposed DPS consumes 186-301 nW while the whole chip consumes 107 mW, resulting in competitive figure of merits of 1.71 nJ/frame · pix and 1.43 e^- · pJ/DRU compared with previous DPSs.**

***Index Terms*—digital pixel sensor, multiple integration, pulse frequency modulation, charge reset, wide dynamic range.**

I. Introduction

Recently, applications of CMOS image sensors (CISs) in automatic driving and computer vision are increasing continually. In such applications, CISs with high-speed and wide-dynamic-range (WDR) imaging capabilities are required to capture high-speed moving objects under various illuminance. Digital pixel sensor (DPS) is proposed to meet the demands of the above applications. Each pixel of DPS contains photo-sensing element together with an analog-to-digital converter (ADC) [1] to execute massively parallel light-to-digital conversion, which realizes high-speed global shutter imaging inherently. The rapid progress of CIS process, particularly backside illumination (BSI) and pixel-level wafer-to-wafer hybrid bonding, has enabled 3D stacked DPSs to achieve significant pixel size reduction [2]–[5]. However, for DPSs based on voltage-mode active pixel sensor (APS), their voltage swing is limited by the supply voltage. With decreasing supply voltage of modern deep-submicron CMOS technologies, the full well capacity (FWC) and dynamic range of DPSs are expected to decrease [6].

One promising solution to achieve WDR under a decreasing supply voltage is to represent image information in the time domain rather than voltage domain. A pulse frequency modulation (PFM)-based DPS, where photocurrent is converted into a digital-pulse signal through multiple self-reset operation, is proposed to achieve dynamic range over 100 dB [7]–[9]. However, the actual dynamic range of PFM that single-frame readout can offer corresponds to the bit depth of in-pixel counter. It suggests that it is not practical to enhance the DR by increasing the bit depth of counter merely, which results in larger pixel pitch. To release this constraint, a ramp threshold voltage is adopted to double the dynamic range with the same bit depth of counter, but its fully non-linear photo-response is unsuitable for afterward image signal processing [10]–[12]. By using column-wise ADC and accumulating multiple sub-frames, respectively, residue quantization [13] and over-integration for error shaping [14] are proposed to enhance the dynamic range with the bit depth of in-pixel counter unchanged. But the cost of additional power consumption from column-wise ADC and lower frame rate remains an issue. In [15], the in-pixel counter is removed and the digital-pulse signal generated in pixel is sent out of the pixel array through address event representation (AER) mechanism, but this method requires complex arbitration periphery and may introduce errors in the particular case of heavy AER bus congestion due to high event activity.

To resolve the trade-offs among dynamic range, pixel pitch and power consumption, this paper proposes a PFM-based digital pixel sensor with dynamically biased multiple integration. The multiple integration enhances the dynamic range without increasing the bit depth of in-pixel counter and introducing additional fixed pattern noise (FPN). The bias current of pixel is adjusted dynamically during the integration to improve the power efficiency. This paper is organized as follows. Section II introduces the conventional PFM-based digital pixel with single integration. Section III presents principles of the dynamically biased multiple integration. Section IV describes the circuit implementation of the proposed DPS. Section V discusses simulation results and comparison. Conclusions are given in section VI.

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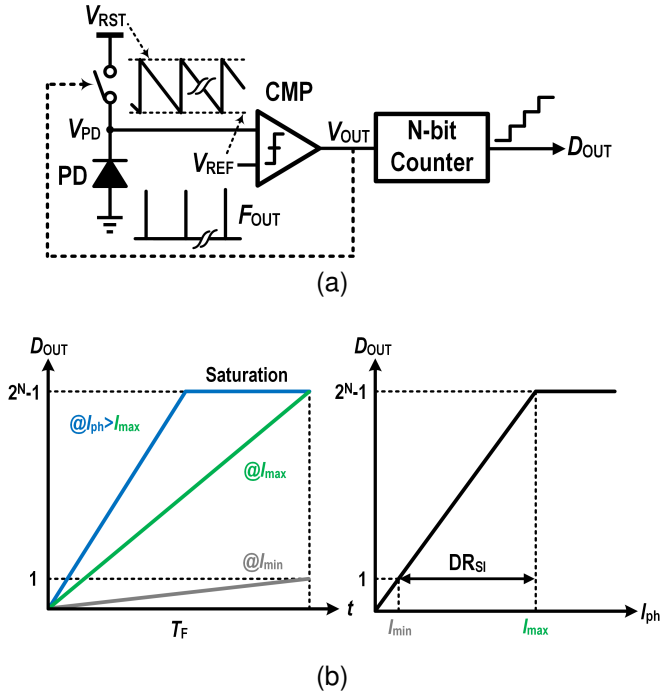


Fig. 1. Conventional PFM-based digital pixel with single integration. (a) Block diagram. (b) Timing diagram and response curve.

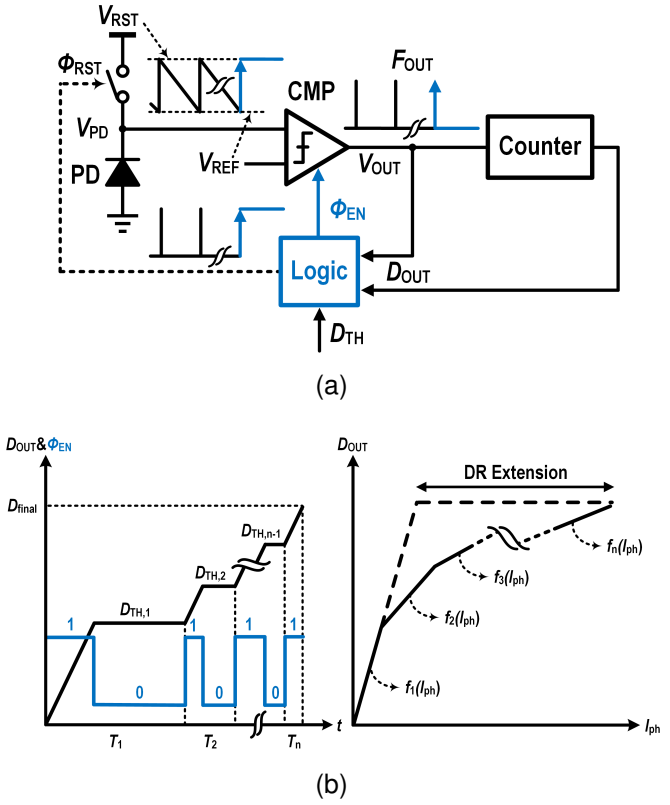


Fig. 2. PFM-based digital pixel with multiple integration. (a) Conceptual block diagram. (b) Timing diagram and response curve.

II. Conventional PFM-based Digital Pixel with Single Integration

The operation of conventional PFM-based digital pixel with single integration is illustrated in Figure. 1. A typical PFM-based digital pixel consists of a photodiode, a reset switch, a comparator and a counter, as shown in Figure. 1(a). $V_{\rm PD}$ gradually decreases as $I_{\rm ph}$ discharges the parasitic capacitance $C_{\rm PD}$ of PD. Once $V_{\rm PD}$ reaches $V_{\rm REF}$, $V_{\rm OUT}$ flips, turning on the reset switch. Thus, $V_{\rm PD}$ is reset to $V_{\rm RST}$. Then $V_{\rm OUT}$ quickly flips again, turning off the reset switch for next discharge. This self-reset operation repeats and generates multiple digital pulses at $V_{\rm OUT}$ whose frequency is determined by $I_{\rm ph}$. $D_{\rm OUT}$ of the following counter increments every time $V_{\rm OUT}$ flips. By counting pulses in a fixed time window, the PFM-based digital pixel serves as a current-to-frequency converter and provides inherent first-order, low-pass filtering. The resulting current-to-frequency conversion can be described for the ideal (zero reset time) case as

$$\begin{aligned} F_{\rm OUT} &= \frac{I_{\rm ph}}{C_{\rm INT}(V_{\rm RST}-V_{\rm REF})} = \frac{I_{\rm ph}}{C_{\rm INT}\Delta V}; \\ D_{\rm OUT}(t) &= F_{\rm OUT}\times t = \frac{I_{\rm ph}t}{C_{\rm INT}\Delta V}. \end{aligned} \tag{1}$$

where $1/V_{\rm INT}\Delta V$ is the sensitivity of the PFM-based pixel. The larger $V_{\rm INT}\Delta V$ is, the less sensitive the pixel becomes. The dynamic range is defined as the ratio of the maximum and minimum detectable photocurrent and is given by

$$\begin{aligned} I_{\rm max} &= D_{\rm OUT}^{-1}(2^N-1); I_{\rm min} = D_{\rm OUT}^{-1}(1); \\ DR_{\rm SI} &= \frac{I_{\rm max}}{I_{\rm min}} = 2^N-1. \end{aligned} \tag{2}$$

Equation (2) indicates that the dynamic range of conventional PFM-based digital pixel is limited by the in-pixel counter. For larger $I_{\rm ph}$, $D_{\rm OUT}$ quickly saturates and becomes indistinguishable, as shown in Figure. 1(b).

III. Proposed Dynamically Biased Multiple Integration

A. Operational Principle of Multiple Integration

The conceptual block diagram of PFM-based DPS with multiple integration is illustrated in Figure. 2(a). Compared with the conventional PFM pixel, a simple logic circuit is added to read the intermediate $D_{\rm OUT}$ for digital threshold detection. Figure. 2(b) illustrates the operation of multiple integration. The whole frame is divided into multiple periods with sequentially decreasing time. $D_{\rm OUT}$ gradually increases as $I_{\rm ph}$ integrates just like the conventional PFM pixel. However, once $D_{\rm OUT}$ reaches the pre-defined digital threshold $D_{\rm TH,i}$ during $T_{\rm i}$, enable signal $\phi_{\rm EN}$ flips from 1 to 0, disabling the comparator and keeping the reset switch on. Therefore, integration of photocurrent as well as pulses counting is stopped. When next integration ($T_{\rm i+1}$) begins, $\phi_{\rm EN}$ returns to 1 and the whole conversion restarts. After repeating the above procedures *n* times, the final result is obtained at the end of the last integration. With the multiple integration, larger $I_{\rm ph}$ can be detectable because $D_{\rm OUT}$ of which does not get saturated. The multiple integration generates continuous piece-wise linear response curve divided into *n* segments with decreasing slope.

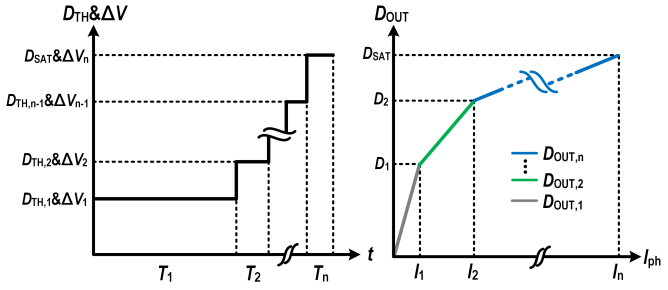


Fig. 3. Digital threshold curve (left) and response curve (right) of the PFM-based DPS with multiple integration.

Wide dynamic range is realized by mapping wide range of I_{ph} into limited range of D_{OUT}.

Since the newly added logic circuit is digital-domain, additional power consumption and FPN of which are negligible. Additionally, the sensitivity of the PFM-based digital pixel can be easily adjustable by just controlling ΔV. With other conditions unchanged, lower sensitivity allows larger I_{ph} detection. Therefore, multiple integration and multiple sensitivity are applied to enhance the dynamic range simultaneously. As illustrated in Figure. 3. gradually increasing $D_{\mathrm{TH,i}}$ as well as ΔV_{i} are assigned to different integration. The relationship between digital threshold curve and response curve of the PFM-based DPS is derived as follow. The maximum counting number $\Delta D_{\mathrm{TH,i}}$ assigned to T_{i} and the ratio of sensitivity as well as time interval of two adjacent integration are defined as

$$\begin{aligned} \Delta D_{\mathrm{TH,i}} &= \begin{cases} D_{\mathrm{TH,i+1}} - D_{\mathrm{TH,i}}, & i > 1, \\ D_{\mathrm{TH,1}}, & i = 1 \end{cases} \\ R_{\mathrm{v,i}} &= \frac{\Delta V_{\mathrm{i+1}}}{\Delta V_{\mathrm{i}}} (i \neq n); \\ R_{\mathrm{t,i}} &= \frac{T_{\mathrm{i}}}{T_{\mathrm{i+1}}} (i \neq n). \end{aligned} \tag{3}$$

(I_{i}, D_{i}) is the coordinates of the breakpoints on the response curve. I_{i} represents the maximum detectable I_{ph} of T_{i}, which is given by

$$I_{\mathrm{i}} = \frac{\Delta D_{\mathrm{TH,i}}}{T_{\mathrm{i}}} \prod_{j=1}^{i-1} R_{\mathrm{v,j}}. \tag{4}$$

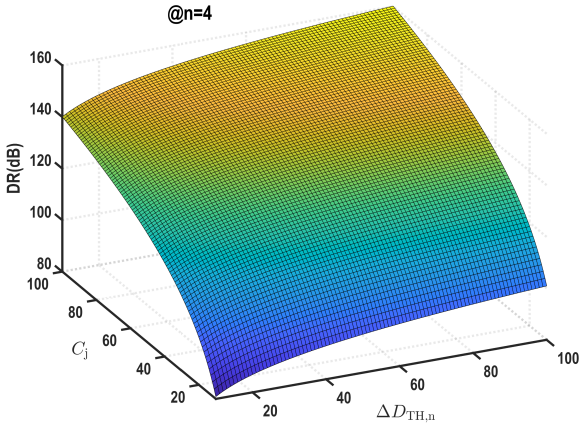
where C_{INT} and ΔV_1 are normalized to one. The expression of $D_{\mathrm{OUT,i}}$ is given by

$$D_{\mathrm{OUT,i}} = I_{\mathrm{ph}} \times \sum_{j=i}^{n} \frac{T_{\mathrm{j}}}{\prod_{k=1}^{j-1} R_{\mathrm{v,k}}} + D_{\mathrm{TH,i-1}}. \tag{5}$$

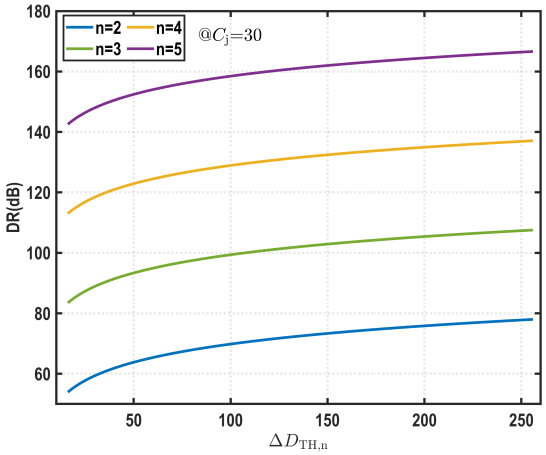
For simplicity, $D_{\mathrm{OUT,i}}$ is assumed to be continuous rather than discrete. By substituting equation (4) into (5), D_{i} is given by

$$D_{\mathrm{i}} = D_{\mathrm{TH,i}} + \Delta D_{\mathrm{TH,i}} \left(1 + \sum_{j=i+1}^{n} \frac{T_{\mathrm{j}}}{\prod_{k=1}^{j-1} R_{\mathrm{v,k}}} \right). \tag{6}$$

The above derivation suggests that if the assignment of $D_{\mathrm{TH,i}}$ and ΔV_{i} are known, the detailed response curve can be calculated. Similarly, for almost any piecewise-linear response curve, $D_{\mathrm{TH,i}}$ and ΔV_{i} are uniquely determined; once the function of response curve is known, $D_{\mathrm{TH,i}}$ and ΔV_{i} can be found by rearranging equation (4)-(6). The dynamic range is defined as the ratio of the maximum and minimum detectable photocurrent. By substituting equation (4)-(5), the dynamic range is calculated as



(a)



(b)

Fig. 4. Dynamic range versus C_{j}, $\Delta D_{\mathrm{TH,n}}$ and n.

$$I_{\max} = I_{\mathrm{n}}; I_{\min} = D_{\mathrm{OUT,1}}^{-1}(1). \tag{7}$$

$$\begin{aligned} DR = \frac{I_{\max}}{I_{\min}} &= \Delta D_{\mathrm{TH,n}} \left(1 + \sum_{i=1}^{n-1} \prod_{j=i}^{n-1} R_{\mathrm{v,j}} R_{\mathrm{t,j}} \right) \\ &= \Delta D_{\mathrm{TH,n}} \left(1 + \sum_{i=1}^{n-1} \prod_{j=i}^{n-1} C_{\mathrm{j}} \right). \end{aligned} \tag{8}$$

where C_{j} is defined as the compression factor. It can be found that *DR* is only related to the maximum counting number of T_{n} rather than other T_{i}. With limited D_{SAT}, larger $\Delta D_{\mathrm{TH,n}}$ improves *DR* at the cost of insufficient resolution for other integration. Calculated results of *DR* with its dependence on C_{j}, $\Delta D_{\mathrm{TH,n}}$ and n are shown in Figure. 4. Assuming all C_{j} are equal, it can be found that *DR* shows stronger dependence

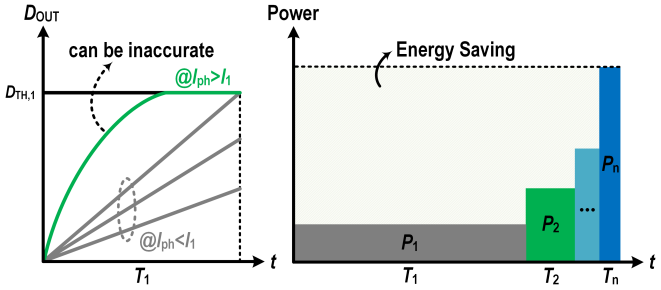


Fig. 5. Illustration of the dynamic bias scheme.

on C_j (or n) than $\Delta D_{TH,n}$ since DR is a power-exponential function of C_j and n.

B. Multiple Integration with Dynamic Bias Current

Indicated by equation (1), the larger I_{ph} is, the higher F_{OUT} is, and the larger power consumption is required to precisely generate F_{OUT}. Each integration corresponds to a certain detectable range of I_{ph}. As illustrated in Figure. 5, for $I_{ph} \in [0,I_1]$, F_{OUT} need to be generated precisely to obtain D_{OUT} without linearity error. However, for I_{ph} larger than I_1, F_{OUT} during T_1 can be inaccurate as long as the intermediate D_{OUT} can reach the digital threshold $D_{TH,1}$. This brings the advantage that power consumption of the proposed DPS can be set at low level at first for detection of smaller I_{ph}. Then the power consumption gradually increases to meet the demand of larger I_{ph}.

It is worth noticing that circuit's bandwidth $F_{BW,i}$ of T_i should match the corresponding maximum output frequency $F_{max,i}$. Therefore, the average power consumption with dynamic bias current is calculated as

$$\begin{aligned} F_{BW,i} \propto g_{m,i} \propto \sqrt{I_{BIAS,i}} \propto F_{max,i}; \\ F_{max,i} = \frac{\Delta D_{TH,i}}{T_i}; \\ P_{aver,db} \propto \frac{\sum_{i=1}^{n} F_{max,i}^2 T_i}{\sum_{i=1}^{n} T_i} = \frac{\sum_{i=1}^{n} \frac{\Delta D_{TH,i}^2}{T_i}}{T_{exp}}. \end{aligned} \tag{9}$$

where $g_{m,i}$ and $I_{BIAS,i}$ are the transconductance and bias current of the circuits, T_{exp} is the total integration time. Without applying dynamic bias current, the power consumption of each pixel has to meet the demand of the last integration and is given by

$$P_{aver,cb} \propto \frac{\Delta D_{TH,n}^2}{T_n^2}. \tag{10}$$

Therefore, the proportion of energy saving due to the dynamic bias current is given by

$$1 - \frac{P_{aver,db}}{P_{aver,cb}} = 1 - \frac{T_n}{T_{exp}} \left(1 + \sum_{i=1}^{n-1} \frac{T_n D_{TH,i}^2}{T_i D_{TH,n}^2} \right). \tag{11}$$

Generally, it can be found that the proportion of energy saving and P_{aver} simultaneously become larger with larger $D_{TH,n}$ and smaller T_n. The detailed assignment of $\Delta D_{TH,i}$ and T_i also affects P_{aver}. For given requirements such as frame rate and dynamic range, optimization for power consumption can be performed based on equation (9).

TABLE I
SPECIFICATIONS OF THE PROPOSED DPS

Parameter	Value
Dynamic Range	>110 dB
Frame Rate	250 fps
Pixel Pitch	21 μm
Array Size	500×500
Pixel Power	⩽0.5 μW
Number of Integration Periods	3
Resolution of Global DAC	5-bit

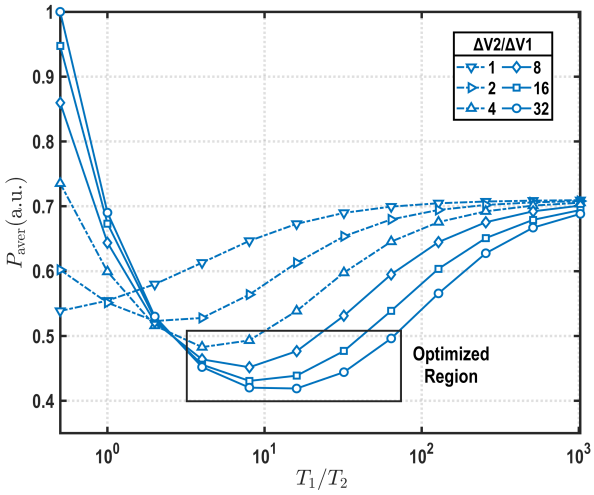


Fig. 6. P_{aver} versus different combinations of $\Delta V_2/\Delta V_1$ and T_1/T_2.

IV. CIRCUITS IMPLEMENTATION

The targeted specifications of the proposed DPS are listed in Table I. In this design, the whole frame is divided into three integration periods to cover a dynamic range over 110 dB while achieving a frame rate of 250 fps. An 8-bit counter is selected due to area constraint. 128, 64, and 63 digital codes are assigned to three segments of the response curve so that each segment has sufficient resolution. An area-efficient 5-bit global digital-to-analog converter (DAC) with less design complicity is adopted to generate ΔV_i (discussed later in section IV-B). With some margin, the following equation should be satisfied to meet the requirements above.

$$\begin{aligned} \frac{\Delta V_3}{\Delta V_1} = 2^5; \\ D_1 = 128; D_2 = 192; \\ \mathrm{DR} = 2^{19}; \sum_{1}^{3} \mathrm{T_i} = 3.6 \text{ ms}. \end{aligned} \tag{12}$$

Different combinations of $\Delta V_2/\Delta V_1$ and T_1/T_2 are substituted to calculate the average power consumption under the constraint of equation (12), as shown in Figure. 6. The calculated result shows that combinations in the optimized region have relatively low average power consumption. Therefore,

$\Delta V_2/\Delta V_1 = 8$ and $T_1/T_2 = 8$ is selected for the following design.

A. Overall Operation of the Proposed DPS

The PFM-based digital pixel with the voltage-reset circuit shown in Figure. 2 is simple, but it poses a strict demand on the comparator. As shown in Figure. 7, the subtracted voltage ΔV_{VR} of voltage reset is related to comparator's delay, offset voltage and I_{ph} since V_{INT} always equals to the fixed V_{RST} after each reset, which results in linearity error. On the other hand, charge reset is better than voltage reset because the subtracted voltage ΔV_{CR} of charge reset equals to the ideal ΔV by controlling the transferred charges ΔQ. Therefore, a charge reset circuit modified from [16] is proposed in this design to guarantee proper operation of the multiple integration.

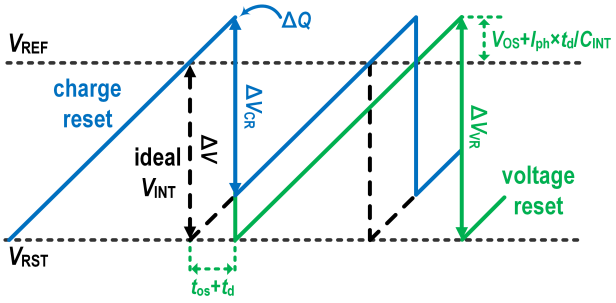


Fig. 7. Comparison of Charge Reset and Voltage Reset.

The block diagram of the proposed DPS is redrawn in Figure. 8. An ac-coupled capacitive transimpedance amplifier (CTIA) and switch-capacitor reset circuit form the analog part; a clocked comparator, reset logic and in-pixel counter form the digital part. A dummy pixel and a replica reference generation circuit are located outside the pixel array, providing reset voltage V_{RST} and initial calibration voltage V_{CAL} for the pixel array. An 8-bit synchronous linear feedback shift register (LFSR) counter [17] is applied for its attractions including: 1) global readout circuits are unnecessary since the counter can be configured as a shift register with a simple readout control circuit; 2) the counter design is simple with a very regular and compact layout.

The operation of the proposed DPS is as follow. At the first auto-zero phase, S_3 and S_4 turn on, storing offset voltage and low-frequency noise of the amplifier at C_{AZ}. S_4 is a low-leakage switch which consists of three transistors. When S_4 turns off, the node between M_1 and M_2 is tied to an external voltage (V_{XM}) close to V_{X}, so the leakage path from V_{X} to V_{INT} is eliminated. V_{PD} and the right plate of C_{INT} are reset to well-defined voltage V_{CM} and $V_{\mathrm{CAL},1}$ respectively. After auto-zero phase, C_{INT} is connected to V_{INT} and the first integration starts from $V_{\mathrm{CAL},1}$. The transimpedance gain is given by

$$\frac{V_{\mathrm{INT}}}{I_{\mathrm{ph}}}(s) = \frac{1}{s\left(\frac{(C_{\mathrm{PD}}+C_{\mathrm{INT}})(1+C_{\mathrm{X}}/C_{\mathrm{AZ}})+C_{\mathrm{X}}}{A} + C_{\mathrm{INT}}\right)}. \quad (13)$$

where C_{PD} is the parasitic capacitance of photodiode, C_{X} and A are input capacitance and open-loop gain of the amplifier. Assuming $C_{\mathrm{X}} \ll C_{\mathrm{AZ}}$, $A \gg 1 + C_{\mathrm{PD}}/C_{\mathrm{INT}}$ and I_{ph} is constant during the whole frame, we have

$$V_{\mathrm{INT}}(t) = \frac{I_{\mathrm{ph}}}{C_{\mathrm{INT}}}t + V_{\mathrm{CAL},1}. \quad (14)$$

When CK=0, V_{RST} is sampled on C_{S}. At each rising edge of CK, V_{INT} is periodically compared with V_{REF}. Once V_{INT} exceeds V_{REF}, $V_{\mathrm{O+}}$ turns low and generates two control signals Φ_{S} and Φ_{RST}, disconnecting C_{S} from V_{RST} and connecting V_{S} to V_{PD}, respectively. As V_{PD} equals to V_{CM} due to the feedback loop, a certain number of charges from C_{S} are transferred to C_{INT} and a voltage subtraction is realized as illustrated in Figure. 7. The subtracted voltage ΔV of each reset is given by

$$\Delta V = \frac{C_{\mathrm{S}}}{C_{\mathrm{INT}}}\left(V_{\mathrm{RST}} - V_{\mathrm{CM}}\right). \quad (15)$$

Equation (15) shows that ΔV depends on the ratio of C_{S} and C_{INT}. It does not contain threshold voltage of transistor, thus showing good uniformity. The digital threshold $D_{\mathrm{TH,i}}$ is inherently set by the number of clock cycles of each integration. By this way, extra circuits for digital threshold detection are eliminated. After first integration, DPS enters auto-zero phase again to set a new bias current and a lower sensitivity as mentioned in section II. The second and third integration repeat the same procedures just like the first integration.

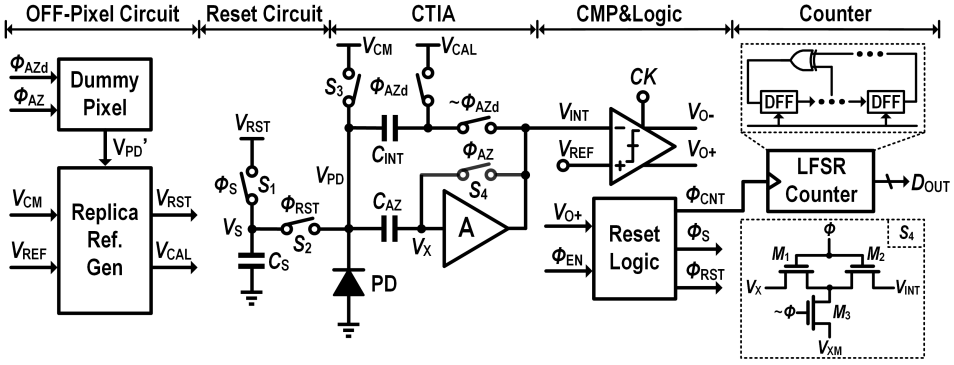


Fig. 8. Block diagram of the proposed DPS.

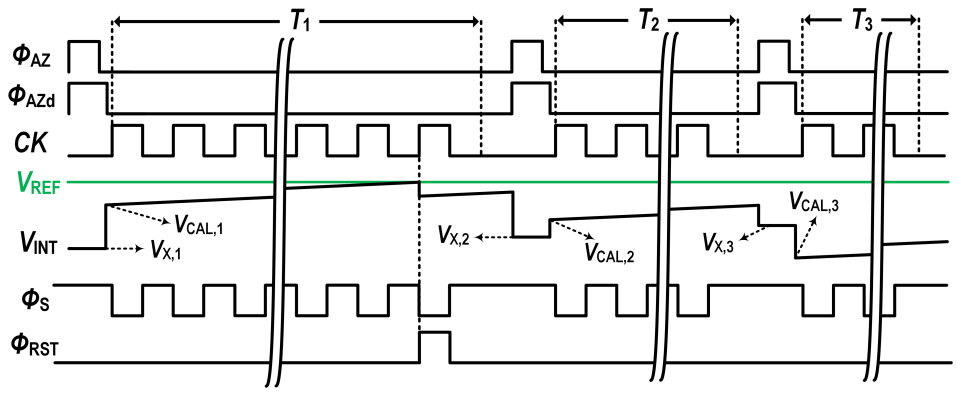


Fig. 9. Timing diagram of the proposed DPS.

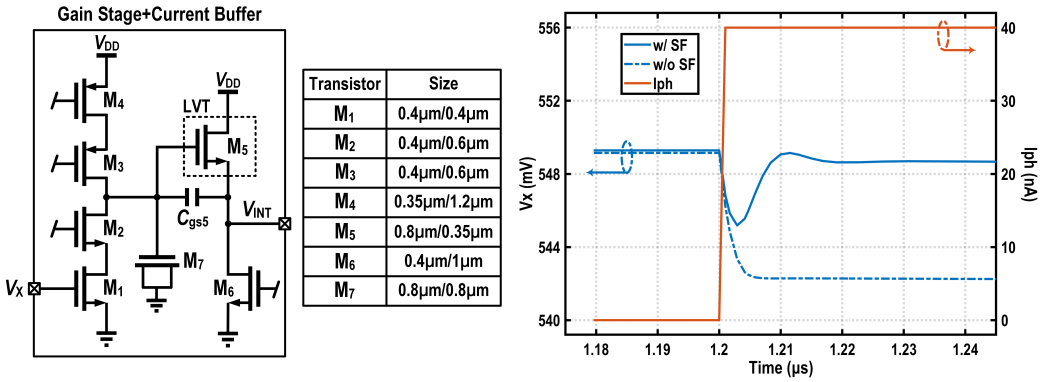


Fig. 10. Schematic and simulated waveform of the adopted amplifier.

B. Error Analysis and Compensation of the Proposed Charge Reset

Based on the principle of this charge reset, it can be found that the source of reset error might include: 1) the inaccuracy of virtual ground at $V_{\rm PD}$ (or $V_{\rm X}$); 2) other unexpected charges except for those from $C_{\rm S}$. Since switched-capacitor circuit and amplifier have been applied, one possible concern is that non-ideal amplifier and channel charge-injection (or clock-feedthrough) of switches might contribute error. Effects of the above non-ideal factor and the corresponding error compensation are discussed in this section.

First, design consideration of the amplifier to ensure accuracy of virtual ground is discussed. Usually, a simple single-ended single-stage cascode amplifier is able to provide enough DC gain for CTIA [18]. However, since the proposed DPS is targeted for WDR imaging, the amplifier needs to output large current for integration of photocurrent. Large output current deviates the amplifier from proper dc operating point and lowers the open-loop gain. Therefore, a single-ended cascode amplifier followed by a source follower (SF) as a current buffer is adopted, as shown in Figure. 10. Voltage ripple at $V_{\rm X}$ under large $I_{\rm ph}$ is given by

$$\begin{aligned}\Delta V_{\rm w/o\ SF} &= \frac{1}{g_{\rm m}} I_{\rm ph};\\ \Delta V_{\rm w/\ SF} &= \frac{\eta C_{\rm gs5}}{g_{\rm m} C_{\rm INT}} I_{\rm ph}.\end{aligned} \tag{16}$$

where $g_{\rm m}$ is the transconductance of $\rm M_1$, η is the body effect factor of $\rm M_5$. As transistor size and bias current of in-pixel amplifier are limited, low $g_{\rm m}$ is expected and thus accuracy of virtual ground is degraded without SF, which causes signal-dependent error. With the help of SF, voltage ripple at $V_{\rm X}$ decreases significantly since η and $C_{\rm gs5}/C_{\rm INT}$ are smaller than one. Transient simulation shown in Figure. 10 was performed to prove the effectiveness of the adopted amplifier. Simulation results shows that voltage ripple of $V_{\rm X}$ is 0.61mV with SF and 6.87mV without SF, respectively, which is consistent with the deduction above.

Another source of reset error is illustrated in Figure. 11. At the falling edge of $\Phi_{\rm AZ}$, channel charges (or clock-feedthrough) $Q_{\rm ch}$ of $\rm S_4$ flows into $C_{\rm AZ}$ while $V_{\rm PD}$ is still connected to $V_{\rm CM}$, resulting in a voltage dip at $V_{\rm X}$ which equals to $Q_{\rm ch}/C_{\rm AZ}$. Then at the falling edge of $\Phi_{\rm AZd}$, the feedback loop is established and forces $V_{\rm X}$ to recover. However, $V_{\rm PD}$ deviates from $V_{\rm CM}$ during the recovery of $V_{\rm X}$ since $V_{\rm PD}$ and $V_{\rm X}$ are both floating points. That is, $Q_{\rm ch}$ of $\rm S_4$ degrades the accuracy of $V_{\rm PD}$. This error introduced by $\rm S_4$ might have a large dispersion since $V_{\rm X}$ varies over PVT variation and $C_{\rm AZ}$ usually has a small capacitance due to area limitation. $\rm S_3$ also contributes $Q_{\rm ch}$ but these charges are absorbed by the amplifier and do not affect $V_{\rm PD}$.

Assuming the transition speed of $\Phi_{\rm S}$ and $\Phi_{\rm RST}$ is fast, when charge reset is activated, $Q_{\rm ch}$ of $\rm S_1$ is split equally to its two terminals. At the same time, $\rm S_2$ absorbs $Q_{\rm ch}$ from $\rm S_1$ and $Q_{\rm ch}$

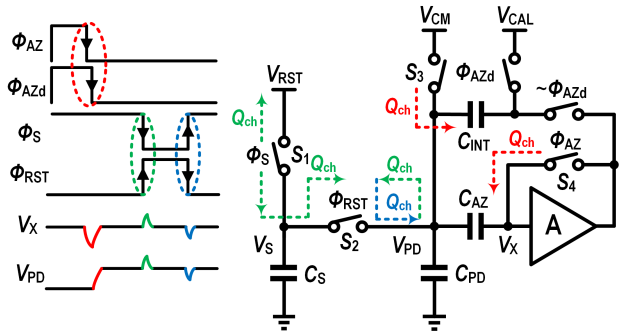


Fig. 11. Illustration of reset error from switches.

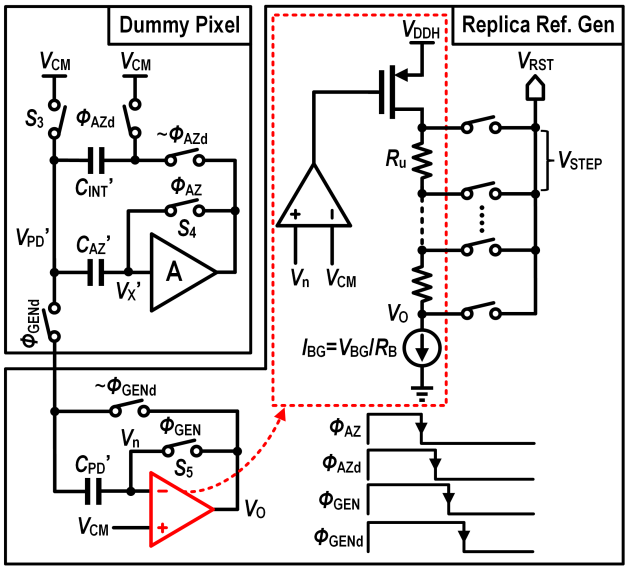


Fig. 12. Schematics of dummy pixel and replica reference generation circuit (compensation network not shown).

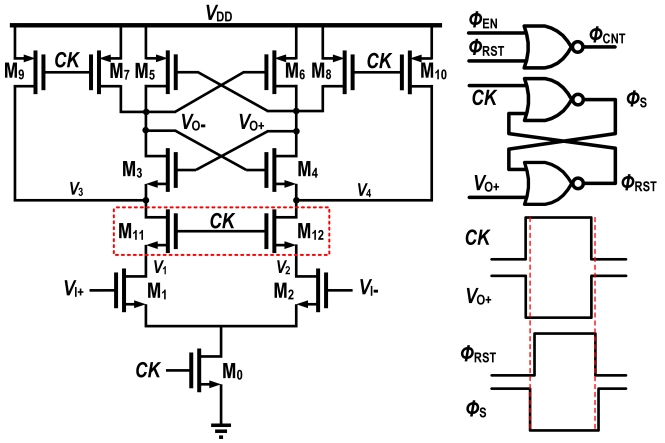


Fig. 13. Schematics of dynamic comparator and logic.

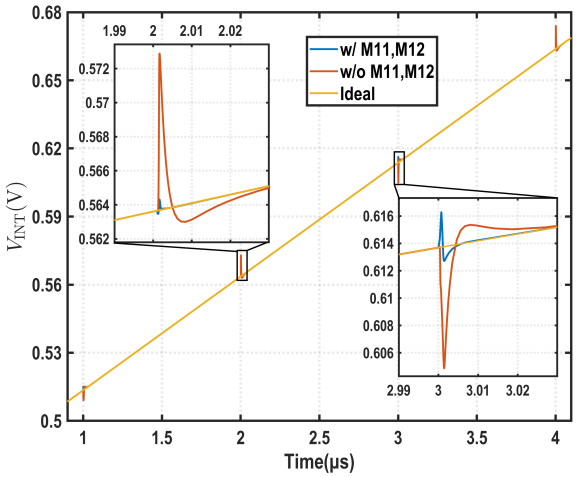


Fig. 14. Reduction of kickback noise by adding transistor M_{11} and M_{12}.

from $V_{\rm PD}$ for channel formation. Therefore, $Q_{\rm ch}$ from S_1 is cancelled but $Q_{\rm ch}$ from $V_{\rm PD}$ introduces a temporary error at $V_{\rm INT}$. Fortunately, when charge reset is finished, S_2 releases $Q_{\rm ch}$ back to $V_{\rm PD}$, compensating charges it absorbs. That is, $Q_{\rm ch}$ of S_1 and S_2 has no significant effects on the accuracy owing to the opposite-directional compensative switching as long as S_1 and S_2 have the same size. It can be concluded that compensation for error introduced by S_4 is required.

Compensation for error from S_4 can be realized by obtaining $V_{\rm PD}$ with error and using $V_{\rm PD}$ with error to generate $V_{\rm RST}$. By this way, both $V_{\rm RST}$ and $V_{\rm PD}$ include error and thus the difference of them is immune to error. As shown in Figure. 12, at the falling edge of $\Phi_{\rm AZd}$, $V_{\rm PD}^{'}$ with error is generated at a dummy pixel outside the pixel array with the same CTIA and control signals. Then $V_{\rm PD}^{'}$ is sampled to $V_{\rm O}$ by an offset-cancelled buffer at the falling edge of $\Phi_{\rm GENd}$. A differential input amplifier embedded with a resistor-ladder DAC is used in this buffer. The voltage step of each resistor on the resistor ladder is given by

$$V_{\rm STEP} = I_{\rm B} R_{\rm u} = \frac{R_{\rm u}}{R_{\rm B}} V_{\rm BG} \tag{17}$$

where $I_{\rm B}$ is generated and copied from bandgap reference circuit. And $V_{\rm RST}$ is given by

$$V_{\rm RST} = V_{\rm PD} + k \times V_{\rm STEP}. \tag{18}$$

where k is the number of resistors between $V_{\rm RST}$ and $V_{\rm O}$. Since temperature coefficient of $V_{\rm BG}$ and the ratio of resistor is nearly zero, $V_{\rm STEP}$ has low temperature coefficient. Therefore, the difference of $V_{\rm RST}$ and $V_{\rm PD}$ is highly stable and adjustable.

C. Comparator Design and Initial Calibration

The schematic of the dynamic comparator and logic is shown in Figure. 13. Transistor M_{11} and M_{12} isolate M_1 and M_2 from M_3 and M_4, reducing voltage swing of V_1 and V_2. Therefore, the kickback noise of comparator is decreased. It is worth noticing that the residual kickback current from comparator can be absorbed by the amplifier, thus it has negligible effect on $V_{\rm INT}$ as shown in Figure. 14. Three NOR gates are used to generate two non-overlap signal $\Phi_{\rm RST}$ and $\Phi_{\rm S}$ as well as the enable signal $\Phi_{\rm CNT}$ of counter. All transistors of this circuit have minimum size for area reduction.

Small transistor size and unbalanced output loading capacitor of dynamic comparator result in large offset voltage. Though this offset voltage can be cancelled by the charge

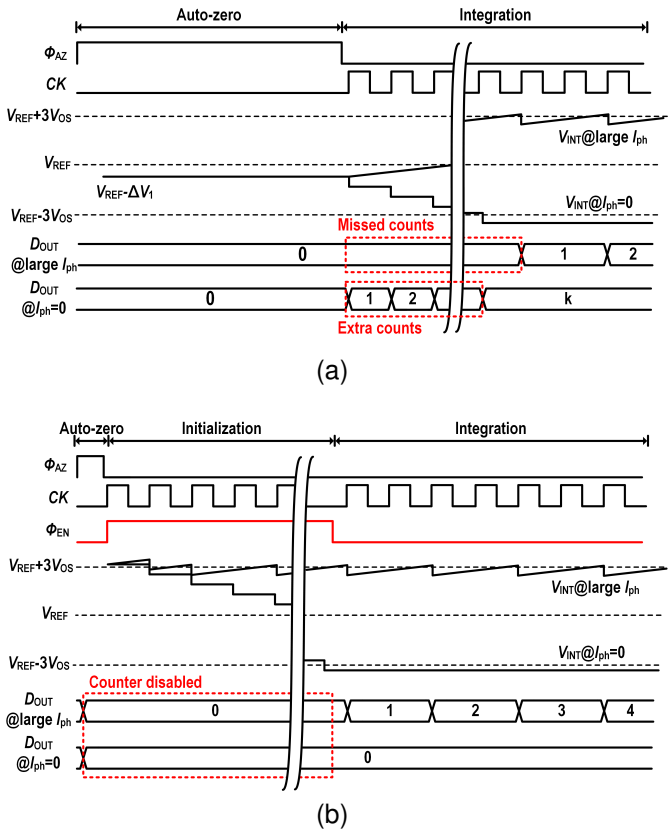


Fig. 15. Timing diagram without (a) and with (b) initialization.

reset, it still affects the digital output before first charge reset is activated. As shown in Figure. 15, ideally, V_{INT} starts increasing from $V_{\mathrm{REF}} - \Delta V_1$, which is slightly below V_{REF} for high sensitivity. Assuming that the actual flip point of the comparator equals to $V_{\mathrm{REF}} + 3V_{\mathrm{OS}}$, even in the case of large I_{ph}, V_{INT} takes a long time to reach the flip point. Therefore, D_{OUT} is less than the ideal value. Similarly, assuming that the actual flip point of the comparator equals to $V_{\mathrm{REF}} - 3V_{\mathrm{OS}}$, even I_{ph} equals to zero, V_{INT} still triggers charge reset repeatedly until V_{INT} is less than the actual flip point. In this case, D_{OUT} is larger than the ideal value.

In order to solve this problem, an initialization is performed before the first integration. V_{INT} is first set to a voltage that is safely larger than all possible flip points and then let the DPS run for several redundant clock cycles to discharge V_{INT} until V_{INT} reaches the actual flip point. During the initialization, the counter is disabled. By discarding several clock cycles before the integration, FPN is effectively reduced.

V. Simulation Results

The layout of the proposed 500×500 DPS are shown in Figure. 16. The digital pixel occupies an area of 21 µm × 21 µm with a fill factor of about 21.5%. C_{S} and C_{INT} are implemented by high density metal-insulator-metal (MIM) capacitors with an area of 1.5 µm × 1.5 µm. Some transistors and routing wires are placed underneath them to save area. V_{REF} and V_{CM} are set to 0.75 V and 0.5 V, respectively. Considering that the maximum voltage swing of V_{INT} is $2\Delta V$,

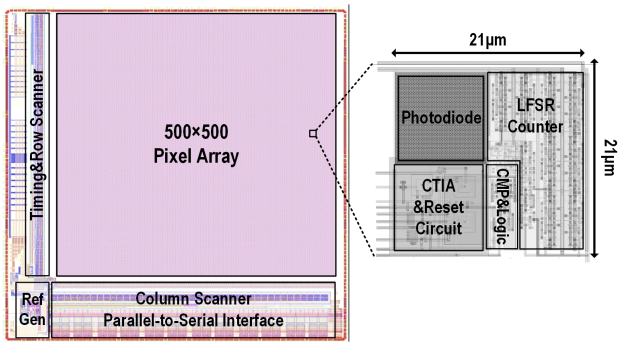


Fig. 16. The layout of the proposed DPS.

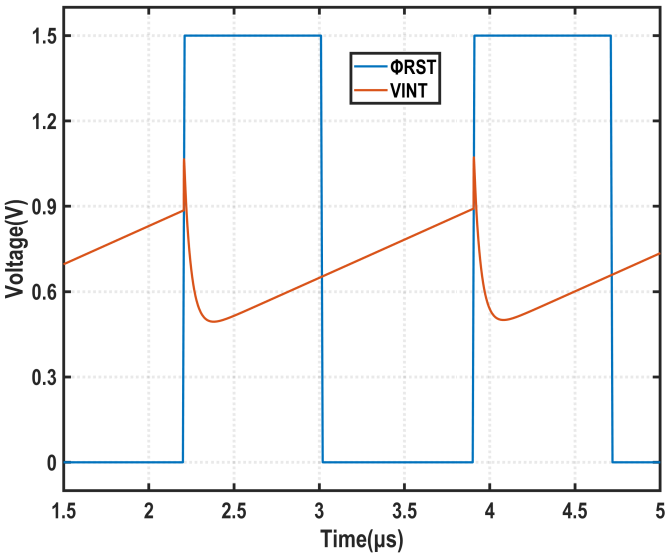


Fig. 17. Simulated waveform of charge reset.

ΔV_1, ΔV_2 and ΔV_3 are set to 15 mV, 120 mV and 480 mV, respectively. The proposed DPS is designed and simulated in a 0.11 µm CMOS process with supply voltages of 2.8/2.2/1.5 V. In this section, netlists are extracted with RC parasitic for post-layout simulation.

As shown in Figure. 17, the charge reset does not block the integration of I_{ph} during reset time. Thus, the output frequency virtually matches the ideal behavior independently of comparator performance as long as reset time is long enough to ensure the complete charge transfer. The PVT simulation was performed with process corner of TT, FF, FS, SF and SS for different power supply(1±10% V_{DD}) and temperature(-40°C-80°C). Herein, the simulation cases are designed as 75 for ΔV_1, ΔV_2 and ΔV_3. Simulation results in Figure. 18 shows that deviation of ΔV_1 is within ±2% with the help of replica reference, which is much lower than that without replica reference. ΔV_2 and ΔV_3 also show a low deviation because ΔV_2 and ΔV_3 are large enough to tolerate error. Since ΔV is related to the sensitivity, the proposed DPS shows good stability on photo-response over PVT variation.

Pixel-to-pixel mismatch is a key metric to pay attention to, as it determines the overall uniformity. To characterize the pixel-to-pixel mismatch of the proposed charge reset, Monte

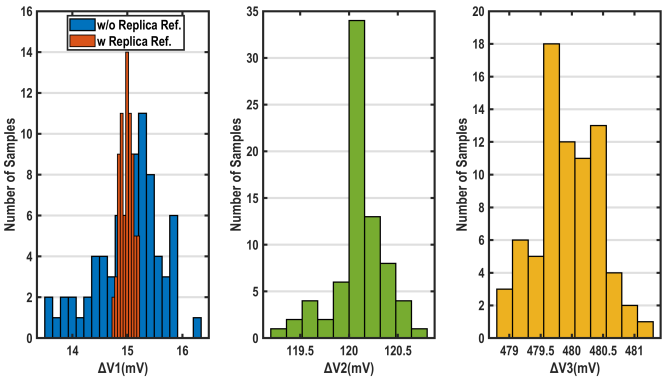


Fig. 18. PVT simulation results of ΔV_1, ΔV_2 and ΔV_3.

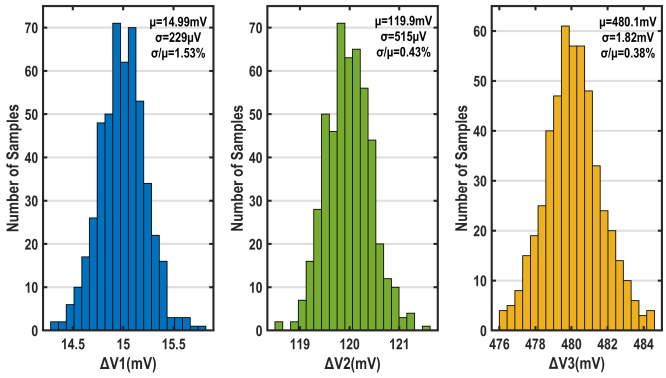


Fig. 19. Monte Carlo simulation results of ΔV_1, ΔV_2 and ΔV_3.

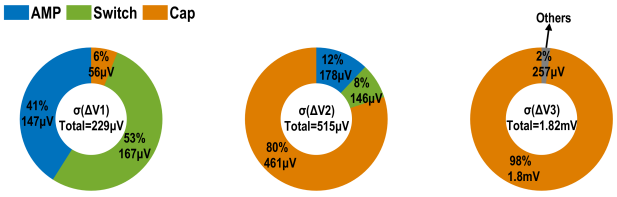


Fig. 20. Proportion of offset voltage of ΔV_1, ΔV_2 and ΔV_3.

Carlo simulation was performed to obtain the offset voltage of ΔV_1, ΔV_2 and ΔV_3. Simulation results in Figure. 19 shows that the offset voltages are 229 μV (1.53%), 519 μV (0.43%), 1.82 mV (0.38%) for ΔV_1, ΔV_2 and ΔV_3, respectively. Figure. 20 illustrates the proportion of offset voltage contributed by switches, amplifier and capacitors. It can be found that there is significant difference between ΔV_1, ΔV_2 (or ΔV_3). For relatively small ΔV_1, error from the non-ideal switches and amplifier is not negligible. Therefore, mismatch of switches and amplifier dominates the offset voltage. For relatively large ΔV_2 (or ΔV_3), error from the non-ideal switches and amplifier is less significant. Therefore, mismatch of C_S and C_{INT} becomes the dominant factor.

The response curve of the proposed DPS is shown in Figure. 21. Compared to conventional single integration, the proposed multiple integration compresses the slope of response curve so that saturation is delayed to larger I_{ph} and thus significantly

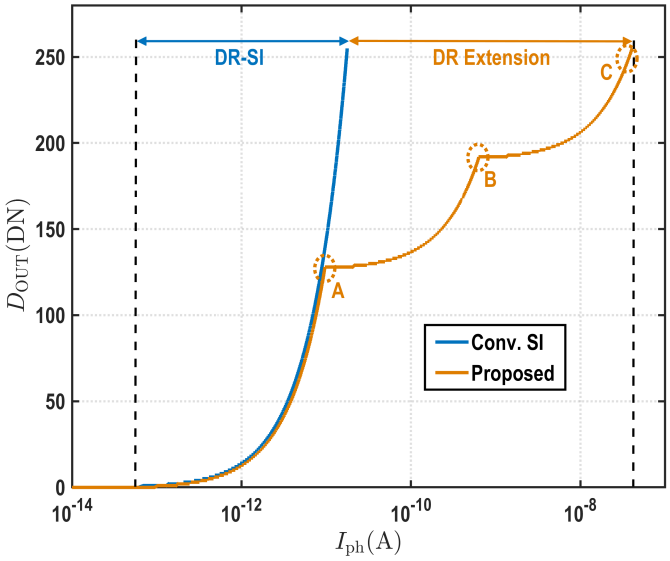


Fig. 21. Transfer curve of the proposed DPS.

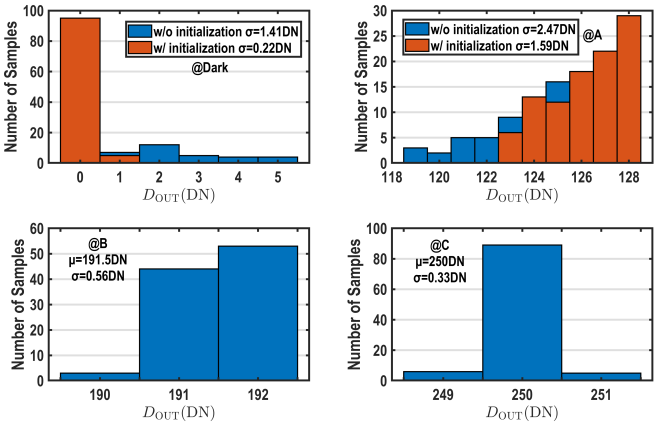


Fig. 22. Monte Carlo simulation results of digital output at different points.

enhances the dynamic range. Monte Carlo simulation was performed to obtain the deviation of D_{OUT} at different points. As shown in Figure. 22, standard deviation of D_{OUT} at $I_{ph} = 0$ is decreased from 1.41 DN to 0.22 DN with initialization which is consistent with the description in section IV-C. Similarly, standard deviation of D_{OUT} at the first breakpoint (point A) is also decreased from 2.47 DN to 1.59 DN. This deviation mainly comes from the offset voltage of ΔV_1.

It should be noted that the distribution of D_{OUT} does not fit normal distribution since its maximum output is limited to 128 for the following reasons: 1) During the first integration, pixels with smaller ΔV_1 due to mismatch obtain higher sensitivity and their D_{OUT} are supposed to be larger. However, since the number of clock cycles assigned to the first integration is fixed, even pixels with higher sensitivity can not obtain larger D_{OUT}. 2) Slope of the response curve decreases at this breakpoint, and a larger step of I_{ph} is required to increase D_{OUT} by one. In summary, the maximum output is limited to 128 for I_{ph} at point A and the FPN at this breakpoint is 1.26%.

The output distributions at point B and C are also shown

TABLE II
PERFORMANCE SUMMARY OF THE PROPOSED DPS

Parameter	Condition	Value
DNL	1^{st} segment	+0.3/-0.3 LSB_1
	2^{nd} segment	+0.2/-0.1 LSB_2
	3^{rd} segment	+0.3/-0.2 LSB_3
INL	1^{st} segment	+0.4/-0.6 LSB_1
	2^{nd} segment	+0.3/-0.1 LSB_2
	3^{rd} segment	+0.5/-0.2 LSB_3
Non-Uniformity	-	$\leqslant$1.5%
Random Noise	@$\sigma(D_{\mathrm{OUT},1})/\mu(D_{\mathrm{OUT},1})$=1	0.47 DN
Dynamic Range	-	120.5 dB
Pixel Power	@$I_{\mathrm{ph}}=0$	186 nW
	@Saturation	301 nW
	w/o dynamic bias current	$>$1.58 µW
Total Chip Power	Pixel Array+Periphery	107 mW

in Figure. 22. The FPN at point B (or C) is smaller than that at point A for the following reasons: 1) the mismatch of ΔV_2 (or ΔV_3) is smaller than that of ΔV_1. 2) the offset voltage of ΔV_2 (or ΔV_3) only acts during the corresponding integration since its D_{OUT} definitely reaches the digital threshold during the preceding integration.

Other parameters of the proposed DPS have been gathered in Table II. The differential nonlinearity (DNL) of each segment is less than 0.3 LSB and the integral nonlinearity (INL) of each segment is less than 0.6 LSB. It should be pointed out that LSB of each segment is different since the slope of each segment is different. Random noise where $\sigma(D_{\mathrm{OUT},1})/\mu(D_{\mathrm{OUT},1})$ equals to one determines the minimum detectable I_{ph}, which is given by

$$I_{\mathrm{min}}=\frac{\sigma(D_{\mathrm{OUT},1})}{\partial D_{\mathrm{OUT},1}/\partial I_{\mathrm{ph}}}. \tag{19}$$

The resulting dynamic range is 120.5 dB, achieving a 65.9 dB extension compared to the conventional single integration. The pixel power varies with I_{ph}. The pixel power at $I_{\mathrm{ph}}=0$ is 186 nW which is dominated by the static current consumption of CTIA while the pixel power at saturation is 301 nW. The extra power consumption mainly comes from the dynamic current consumption for integration of photocurrent, charge reset and counter's counting. Pixel power without applying dynamic bias current is at least 1.58 µW. These results verify the effectiveness of the dynamic bias scheme on improving energy efficiency. Other periphery circuits including row/column scanners, timing/reference generation and I/O buffers consume 46 mW, resulting in a total chip power of 107 mW.

Table III shows the major metrics of the proposed DPS compared with previous DPSs. The figures of merit (FOM) is computed based on the following formula used in [23].

$$\mathrm{FOM}_1=\frac{\text{Chip Power}}{\text{Array Size}\times\text{Frame Rate}} \tag{20}$$

$$\mathrm{FOM}_2=\frac{\text{Chip Power}\times\text{Random Noise}}{\text{Array Size}\times\text{Frame Rate}\times\text{Dynamic Range}} \tag{21}$$

DPS in [19], which is fabricated in advanced stacked CIS process, achieves the smallest pixel pitch and the lowest FOM. Compared with those DPSs fabricated in similar CMOS process [15], [20]–[22], the proposed DPS achieves wide dynamic range while maintaining reasonable frame rate and pixel pitch, resulting in more balanced and lower FOMs of 1.71 nJ/frame $\cdot$ pix and 1.43 $\mathrm{e}^-\cdot$pJ/DRU, respectively.

TABLE III
COMPARSION WITH PRIOR DPSS

Reference	[19]	[15]	[20]	[21]	[22][a]	This work[a]
Process	45/65nm stacked	0.18 µm	0.35µm	0.18µm	0.18µm	0.11µm
Array Size	512×512	96×128	180×148	128×128	640×512	500×500
Fill Factor	/[b]	10%	7%	/[b]	/[b]	21.5%
Pixel Pitch(µm)	4.6	25	33	15	15	21
Non-Uniformity	47e^-	2.6%	1.8%	N.A.	N.A.	$\leqslant$1.5%
Chip Power(mW)	5.75	58.5@100fps	4.5	13.88	18.74	119.5
Frame Rate(fps)	30	0.1-200	0.125	200	120	250
Dynamic Range(dB)	127	130@0.1fps 125@3fps 105@30fps	151	99.2	101	120.5
FOM_1(nJ/frame $\cdot$ pix)	0.73	47.7	1352	4.24	0.47	1.71
FOM_2($\mathrm{e}^-\cdot$pJ/DRU)	0.0014 (w/ FPN correction) 0.18 (w/o FPN correction)	N.A.	0.95	10.22	4.65	1.43

[a]Simulation results; [b]Photo-sensing area not included or located at another layer.

VI. Conclusion

This paper presents a wide-dynamic-range PFM-based DPS with dynamically biased multiple integration. While multiple integration enhances the dynamic range by sequentially compressing the photo-response curve, a dynamic bias scheme is proposed for energy saving. Furthermore, stable and uniform photo-response of the proposed DPS is realized by the modified charge reset circuit with error compensation. The proposed DPS achieves a dynamic range of 120.5 dB with pixel power of 186-301 nW. Compared with previous DPSs, competitive figure of merits of 1.71 nJ/frame $\cdot$ pix and 1.43 $e^- \cdot$ pJ/DRU are obtained.

Acknowledgments

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