Energy-efficient switching method using input-swapping for high resolution SAR ADCs

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March 31, 2023

Abstract

This paper presents an energy-efficient digital-to-analog converter (DAC) switching method with low common-mode variations for high resolution successive approximation register (SAR) analog-to-digital converters (ADCs), while enabling to implement resolutions such as 14-bit as compared to the typical 10-bit. The proposed switching method enables high resolution by having a nearly constant common-mode voltage and employing input-swapping to use the reference voltage (Vref) only in the sampling phase. This method eliminates the need for the third reference voltage during the entire DAC switching steps, which reduces the required number of switches even compared to the state-of-the-art methods that use low number of switches. The use of lower number of switches not only lowers the DAC control logic complexity, but also results in a faster operation, lower power, and smaller area. When compared to conventional 10-bit SAR ADCs, the proposed switching method in a 10-bit implementation reduces the average switching energy and area by 93.7 % and 75 %, respectively, while offering high resolution implementation options such as 14 bits.

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This paper presents an energy-efficient digital-to-analog converter (DAC) switching method with low common-mode variations for high resolution successive approximation register (SAR) analog-to-digital converters (ADCs), while enabling to implement resolutions such as 14-bit as compared to the typical 10-bit. The proposed switching method enables high resolution by having a nearly constant common-mode voltage and employing input-swapping to use the reference voltage (V_{ref}) only in the sampling phase. This method eliminates the need for the third reference voltage during the entire DAC switching steps, which reduces the required number of switches even compared to the state-of-the-art methods that use low number of switches. The use of lower number of switches not only lowers the DAC control logic complexity, but also results in a faster operation, lower power, and smaller area. When compared to conventional 10-bit SAR ADCs, the proposed switching method in a 10-bit implementation reduces the average switching energy and area by 93.7 % and 75 %, respectively, while offering high resolution implementation options such as 14 bits.

Introduction: Successive approximation register (SAR) analog-to-digital converters (ADCs) have been widely used in recent years in many applications that require low-power consumption and medium resolution such as 10-bit. There is a constant effort in literature to lower the power consumption of the SAR ADCs even further while increasing their resolutions. A large portion of the power consumption in the SAR ADCs comes from the switching power of the DACs. Recent studies in the SAR ADCs have focused on the switching

power reduction of the DACs with different methods [1-6] compared to the conventional approach, but all of these methods have different drawbacks. The set-and-down switching method in [1] achieves 99.3% reduction in the average switching energy at the expense of large common-mode voltage variation that degrades the performance of the comparator, which is the main factor determining the resolution. The bi-directional switching method in [2] can provide higher resolution as it reduces the common-mode variations by using a single-side capacitor switching; however, this method consumes high reset energy, increasing the power consumption. The V_{CM}-based charge-recovery switching method in [3] eliminates the reset energy, but it needs extra voltage reference compared to the conventional switching method, which increases the power consumption and requires large silicon area due to the need for the increased number for unit capacitors compared to the state-of-the-art methods; the stability of this third reference voltage is also a concern for the high-resolution implementations in this method. The two-step switching method in [4] reduces the required number of unit capacitors significantly, reducing the area of the unit capacitors; however, this method increases the complexity of the DAC control logic due to the additional circuits, preventing its use in high resolution SAR ADCs. The merge and split switching method in [5] achieves great reduction in average switching energy by creating floating nodes instead of using a third reference voltage, but this approach can lead to linearity problems, limiting its use in high resolution SAR ADCs. The proposed method in [6] needs a very small number of unit capacitors and therefore reduces the switching energy by about 99.5% compared to conventional SAR ADCs. However, this method requires V_{REFN}, V_{REFP}, and V_{CM} to perform the conversion, and again the third reference voltage can seriously degrade the resolution performance of the ADCs. The proposed scheme in [7] divides the input differential voltage by 2 to reduce the power, but demands a better comparator to resolve small voltages, i.e., limiting the ADC resolution. Except the proposed methods in [3] [6], and [7], the above methods use top plate sampling which can degrade the linearity performance due to non-linear parasitic and non-linear clock feedthrough effects. There is a need for a new switching method for achieving high resolution and lower power SAR ADCs. This paper presents a novel switching method by using input swapping with bottom plate sampling and low common-mode variation. The proposed method achieves 93.7% reduction in switching energy and decreases the area by 75% compared to the conventional switching method used in conventional SAR ADCs with a typical 10-bit resolution, while allowing high resolution implementations such as 14 bits.

Fig. 1 shows the proposed 10-bit SAR ADC architecture, which employs a coarse and a fine comparator. Before starting the actual sampling on the main DAC array, first comparison is performed by the coarse comparator to determine whether the differential input is positive or negative. Depending on the result of this first comparison, the DAC arrays are connected to the input voltages, and actual sampling is initiated. At the same time, the output of the fine comparator is also adjusted according to the output of the first comparison. At the end of the sampling, 7 clock cycles are required for the conversion to determine remaining bits of the output. In addition, the proposed scheme split the MSB capacitor into binary-weighted sub-capacitors in the DAC array to remove the reset voltage.

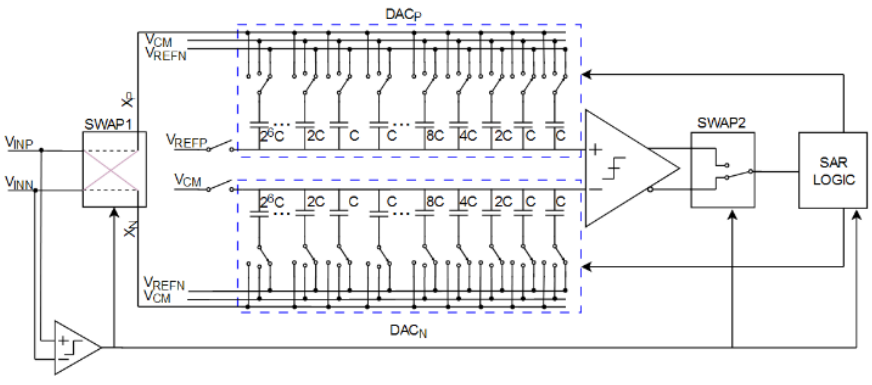
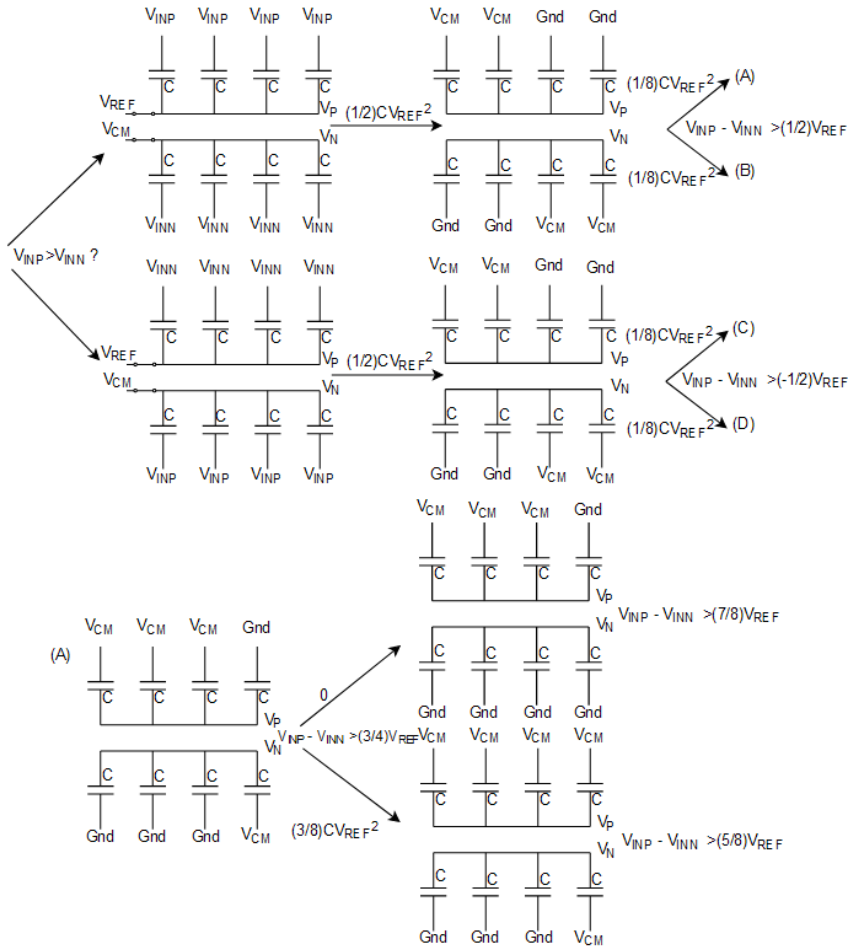
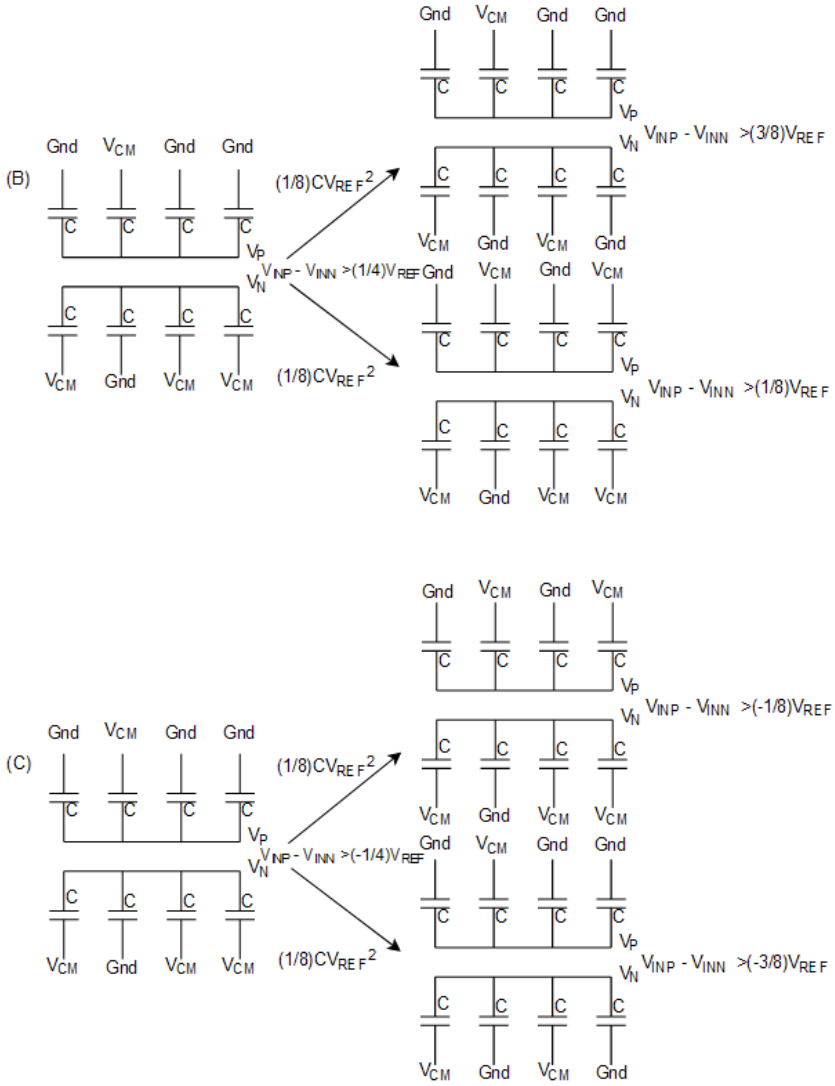


Fig. 1. Proposed 10-bit SAR ADC architecture

Proposed switching method: In the conventional switching method, there are 2^{N+1} unit-capacitors, where N represents the resolution; each of the capacitors, except the dummy capacitor, switches to either V_{REFP} or V_{REFN},requiring large amount of switching energy. In addition to switching energy, reset energy is required to switch back the capacitors to previous voltage in the intermediate cycles. As a result, the switching energy is very large and wasted. The switching energy can be reduced with the proposed method in this paper, by using either common-mode voltage V_{CM} or V_{REFN}, while V_{REFP} is only used in the sampling process. This method also reduces the total number unit capacitors to 2^{N-1}. In addition, the number switches connected to the bottom plate of each capacitor is also reduced compared to the conventional switching method, which lowers the DAC control logic complexity and decreases the settling time of each capacitor due to the reduction in the switches.

Fig. 2 explains the proposed switching scheme for a sample 4-bit SAR ADC. The proposed scheme starts the sampling phase in which the input signal is sampled on the bottom plates of the capacitors, while the top plates of all capacitors are connected to either V_{REF} or V_{CM}. At the end of the sampling phase, the bottom plate of the MSB capacitor, which is split into sub-capacitors, is connected to V_{CM}, while the bottom plates of the remaining capacitors are connected to ground in the DAC_P array. In contrast, in DAC_N the bottom plate of the MSB capacitor is connected to ground while the bottom plates of the remaining capacitors are connected to V_{CM}. After the MSB capacitors are settled to the required voltages, a comparison is performed. If the differential input voltage is greater than V_{CM}, in the next conversion cycle, the bottom plates of (MSB-1) capacitors are connected to V_{CM} and ground. On the other hand, if the differential input voltage is smaller than V_{CM}, the bottom plates of the largest capacitor in the MSB capacitor returns to previous voltage and no changes occur at the bottom plates of the (MSB-1) capacitor. The conversion continues until the last conversion. In the last conversion, according to the result of the previous conversion, one DAC does not change while the bottom plate of the LSB capacitor in the other DAC is connected to either ground or V_{CM}. During the entire DAC switching, only V_{CM} and ground are used to perform the conversion. A third reference voltage called as V_{REF} is not used during the entire switching steps. As a result, the precision of the switching becomes better and does not depend on the accuracy of the third reference voltage.





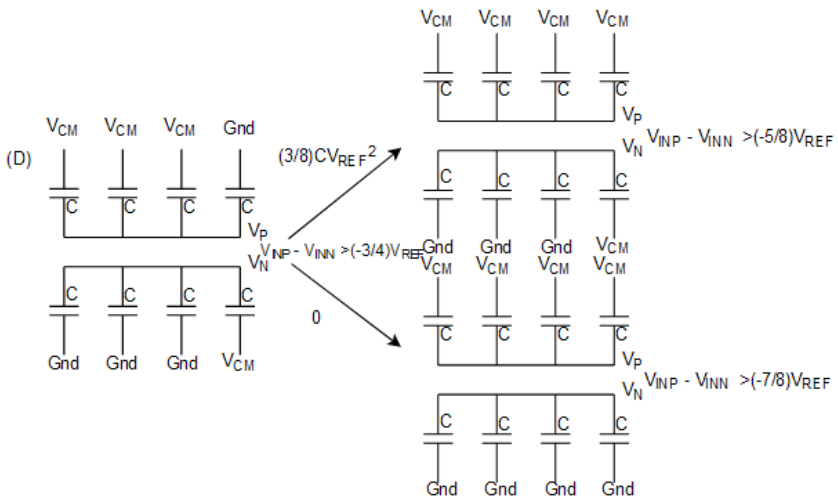
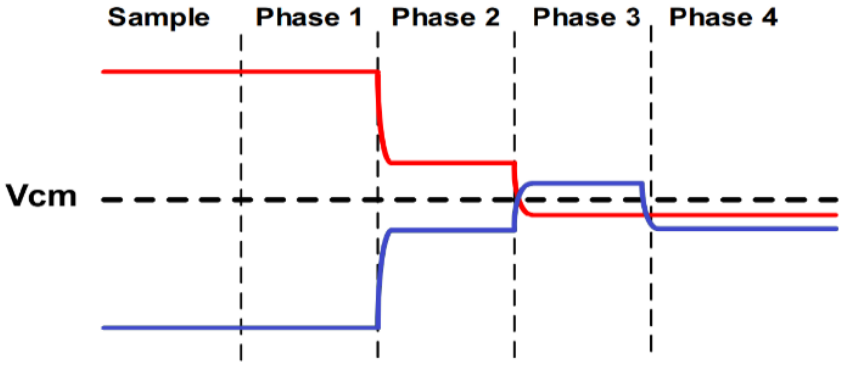


Fig. 2 Proposed switching scheme for 4-bit SAR ADC

Fig. 3 shows the waveform of the proposed DAC scheme for 4-bit switching. The common-mode voltage has minor change in the last conversion which can be tolerable for the comparator. Therefore, the proposed scheme sustains the common-mode voltage nearly constant which provides good CMRR for the comparator while achieving good switching energy efficiency compared to the state-of-the-art methods. In addition, the number of switches required for switching scheme is reduced which does not need complex DAC control logic and signals.



Switching energy comparison: The proposed scheme reduces the switching energy by 93.7% and area by 75% while eliminating the third reference voltage, lowering the complexity of the DAC control logic and reducing the number of switches to implement the DAC scheme. Table 1 summarizes the results and compare the proposed scheme with the state of the art. The proposed scheme provides good energy reduction while having nearly constant common-mode voltage and eliminating the third reference voltage during the entire switching scheme which relaxes the driven ability of V_{REF}. In addition, the bottom plate sampling method is used to eliminate the non-linearity effects coming from the input switches and parasitic. Thanks to the novel technique called as input-swapping, the V_{CM} and V_{REF}switches are connected to DAC_P and $DAC_N$and the charge injection due to these switches only cause static errors which can be corrected by simple correction algorithms.

Table 1. Comparison of the proposed method with published techniques for 10-bit resolution

Switching method	**Switching energy (CV^2)**	**Energy saving (%)**	**Area reduction (%)**	**Extra reference vo**
Conventional	1363.3	0	0	No
Monotonic[2]	255.5	81.2	50	No
Bi-directional [8]	234.2	82.9	75	Yes
V_{cm}-based[6]	170.2	87.54	50	Yes
Split-cap [9]	425.7	68.8	0	No
CAS [10]	344.1	74.8	50	No
Tri-Level [11]	42.42	96.9	**75**	No
Work in [12]	28.8	97.9	75	Yes
Proposed scheme	**85.7**	**93.7**	**75**	No

Conclusion: This paper proposes an energy efficient switching method for SAR ADCs while eliminating the third reference voltage during the entire switching steps by using a novel technique called as input-swapping. Bottom plate sampling is used to prevent non-linearity and non-linear clock feedthrough effects. The proposed switching method achieves energy reduction by eliminating the MSB capacitors used in the conventional method, and splitting the MSB capacitor into sub-capacitor arrays. Compared to the conventional method, the proposed method reduces the energy by 93.7% in a typical 10-bit implementation. The proposed method can be easily used for high resolution applications, like 14-bit.

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