Design and FPGA Implementation of pre-computation based radix-4 hyperbolic CORDIC for Direct Digital Synthesis

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Abstract

This paper presents the hardware and delay efficient design of a radix-4 pipelined hyperbolic Coordinate Rotation Digital Computer (CORDIC) architecture. The proposed design uses pre-computation based micro-rotation sequence generation to reduce the cycle time and number of iterations. It also eliminates the need for residue angle computation in every iteration that helps to enhance the operating speed. The methodology finds a linear relation between rotation angle input and micro-rotation sequence by selectively choosing elementary angles from the set of valid angles. Therefore, it requires six clock cycles to compute the hyperbolic functions ($cosh/sinh$). Further, the region of convergence (ROC) of the proposed design is extended to cover the entire coordinate space. Based on the proposed hyperbolic CORDIC design, a hyperbolic (Direct Digital Synthesis) DDS is implemented using **XC7VX330T (Vertex-7 family)** field-programmable gate array (FPGA) in Xilinx ISE 14.4 platform. The proposed design achieves **47%** and **37%** savings in basic logic elements and number of slices respectively than recent designs. The design also achieves an improved slice delay product of **5.28** and a maximum frequency of operation of **500.75MHz**.

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