Design of a 21-level multilevel inverter with minimum number of devices count

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Abstract

Multilevel inverters (MLIs) have attracted the attention of researchers for their needs in industrial applications, renewable energy systems, and electric vehicles. MLIs require a large number of power electronic components to synthesize higher levels at the output voltage. However, overuse of power electronic devices increases the complexity, losses, and cost of MLIs. In this study, a new MLI has been proposed with a reduced number of power switches. The basic unit of the proposed MLI comprises only three independent DC sources and ten switches (eight unidirectional, and two bidirectional) to produce 21 levels at the output voltage waveform. The nearest level control (NLC) modulation method has been used to produce gate pulses. Furthermore, three extension topologies have been proposed to generate a higher number of levels and the extension parameters have been compared with recently introduced and conventional topologies. The comparative study shows that the proposed MLI topology requires fewer components in terms of power electronics parameters than the others. On the other hand, the presented first extension study can be used for all non-extendable basic units is one of the prominent values of the study. Simulation studies showing modulation methods, switching patterns, and signal outputs were performed with Matlab/Simulink. A prototype of the proposed main module has been realized and tested in the laboratory with an FPGA processing board. Experimental results have been verified with simulation results, and the performance of the proposed topology has been proven.

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ARTICLE TYPE

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Summary

Multilevel inverters (MLIs) have attracted the attention of researchers for their needs in industrial applications, renewable energy systems, and electric vehicles. MLIs require a large number of power electronic components to synthesize higher levels at the output voltage. However, overuse of power electronic devices increases the complexity, losses, and cost of MLIs. In this study, a new MLI has been proposed with a reduced number of power switches. The basic unit of the proposed MLI comprises only three independent DC sources and ten switches (eight unidirectional, and two bidirectional) to produce 21 levels at the output voltage waveform. The nearest level control (NLC) modulation method has been used to produce gate pulses. Furthermore, three extension topologies have been proposed to generate a higher number of levels and the extension parameters have been compared with recently introduced and conventional topologies. The comparative study shows that the proposed MLI topology requires fewer components in terms of power electronics parameters than the others. On the other hand, the presented first extension study can be used for all non-extendable basic units is one of the prominent values of the study. Simulation studies showing modulation methods, switching patterns, and signal outputs were performed with Matlab/Simulink. A prototype of the proposed main module has been realized and tested in the laboratory with an FPGA processing board. Experimental results have been verified with simulation results, and the performance of the proposed topology has been proven.

KEYWORDS:
Multilevel Inverter, FPGA Implementation, Nearest Level Control, Reduced Switch Count

1 | INTRODUCTION

DC-AC power conversion is essential for applications that draw the current from DC power sources in AC form. Nowadays, inverters have a wide range of applications for high-power operation systems. Many medium-voltage applications such as photovoltaic systems, wind farms, static synchronous compensators (STATCOM), flexible alternating current transmission systems (FACTS), electric vehicles (EVs), AC motor drives, and renewable energy sources (RES) need DC-AC power conversion to operate under AC load conditions [1,2].

[0]**Abbreviations:** ANA, anti-nuclear antibodies; APC, antigen-presenting cells; IRF, interferon regulatory factor

Multi-level inverters (MLIs) are being substituted for traditional inverters because of their many well-known advantages such as high-quality harmonic profiles, low voltage across switches, low electromagnetic interference (EMI), and high efficiency[3]. Advances in power electronics have influenced the evolution of MLI topologies[4]. The higher the output level, the greater the number of power supplies and switches used, increasing the cost, control complexity, and volume. Therefore, researchers focused on creating new hybrids by combining the superior features of different topologies. Traditional MLIs are grouped into three main groups called neutral point clamped (NPC)[5], flying capacitor (FC)[6], and cascaded H bridge (CHB)[7,8]. All conventional topologies can be expanded to synthesize the desired level at the output, but these are some disadvantages[9,10]. CHB topology requires multiple independent DC voltage sources and more switches for higher output levels, while FC topology creates voltage balancing problems and control complexity due to a large number of increased capacitors. Thus, the control will become more complex when the number of capacitors increases for generating higher output voltage levels.

MLIs consist of an arrangement that may have power switches, diodes, DC voltage sources, and DC link capacitors for generating a higher number of voltage levels at the output. The design of MLI topologies depends on the number of voltage levels, total harmonic distortion (THD), modularity, extension model, total standing voltage (TSV), and the number of power components such as power switches, DC sources, diodes, capacitors, etc.[11]. Researchers have focused on new MLI topologies with a lower number of power components to overcome the shortcomings of traditional topologies[12,13,14,15,16,17,18,19].

In[15], a new cascaded MLI topology is proposed in order to increase the number of output voltage levels with a lower number of power switches. An algorithm is proposed to determine the magnitudes of the DC voltage sources. In this study, it is noted that the proposed topology only uses one-way power switches. A single-phase cascaded MLI is proposed in[18]. The proposed inverter is composed of the series connection of the H-bridge basic units. Authors have presented nine different algorithms to determine the magnitude of DC voltage sources. Two other MLIs have been also presented in[20] and[21]. These two structures can generate positive and negative levels at the output without the need for an H-Bridge. Using the proposed main structure, modular and cascade expansion topologies have been proposed to synthesize higher levels at the output.

In[22], the cascaded MLIs have been investigated and focused on topologies with asymmetric configurations. They reported that to provide a large number of output levels with the same number of inverters, asymmetric MLIs can be used. Thus, they have proposed an asymmetrical cascade MLI topology with reduced switch count and DC voltage sources. Although the asymmetric configuration in the traditional CHB topology requires fewer power switches than the symmetric configuration, the researchers focused on investigating topologies that require fewer switches. Another asymmetric topology is proposed in[23] about two years later. In this study, the authors proposed cascading topology with series-connected DC sources instead of CHBs as in the traditional CHB topology. One of the main constraints in this topology is requiring an H-bridge at the backend of the circuit and therefore require the use of high voltage rating power switches.

In this study, the proposed 21-level topology does not require H-Bridge at the output to reduce the number of power switches and port drivers. The main module comprises 10 power switches (two bidirectional and 8 unidirectional) and 3 DC sources. It is suitable to work in different frequency and modulation index. Three different expansion methods have been presented with the main module to synthesize higher voltage levels at the output voltage waveform. The symmetric and asymmetric modes of the proposed topology are compared with conventional and recently proposed MLI topologies, and the same number of levels at the output voltage are synthesized with fewer power components. The paper has been organized as follows: a detailed analysis of the proposed main module and module configuration is carried out in section II. Section III introduces the extension topologies for generating a higher number of levels at the output voltage. Section IV provides a comparative study of the proposed topology with other MLIs considering power circuit parameters and TSV. The nearest level control modulation technique that is applied to the proposed main module for producing gate driver pulses is presented in Section V. Section VI gives a detailed power loss analysis. Simulation and experimental studies are performed in Section VII. And finally, the conclusions are presented in Section VIII.

2 | PROPOSED TOPOLOGY

2.1 | Basic Module

The main module of the proposed 21-Level MLI is shown in Figure 1. It is composed of two parts, the first part consists of surrounding switches S_{H1}-S_{H4} operating at high frequency, while the switches in the second part operate at lower frequencies. Further, It can generate 21 levels at the output voltage waveform with 3 DC sources and 10 power switches. According to switching modes, it can be seen that the current changes direction in different switching modes on the $S_3 - S_4$ switches. In all

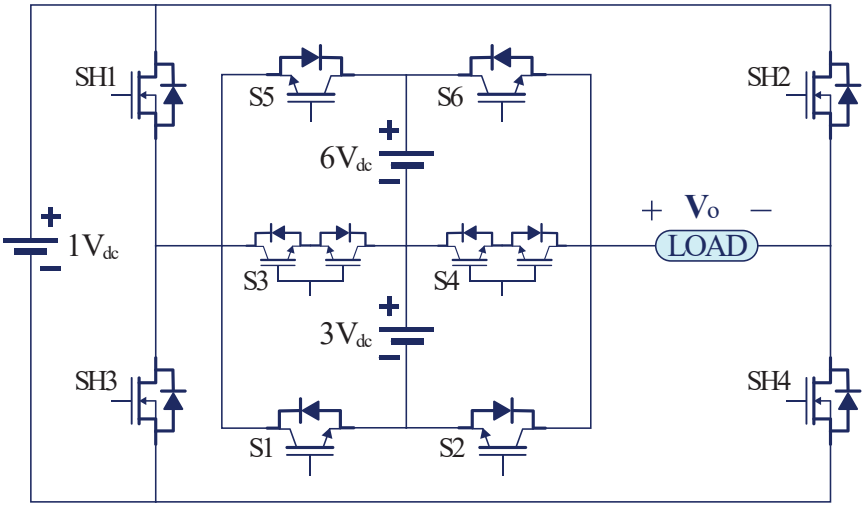


Figure 1 Proposed basic unit.

Table 1 Switching Pattern of Basic Unit

S_1	S_2	S_3	S_4	S_5	S_6	S_{H1}	S_{H2}	S_{H3}	S_{H4}	V_o
1	0	0	0	0	1	1	0	0	1	**10 V_{DC}**
1	0	0	0	0	1	0	0	1	1	**9 V_{DC}**
1	0	0	0	0	1	0	1	1	0	**8 V_{DC}**
0	0	1	0	0	1	1	0	0	1	**7 V_{DC}**
0	0	1	0	0	1	0	0	1	1	**6 V_{DC}**
0	0	1	0	0	1	0	1	1	0	**5 V_{DC}**
1	0	0	1	0	0	1	0	0	1	**4 V_{DC}**
1	0	0	1	0	0	0	0	1	1	**3 V_{DC}**
1	0	0	1	0	0	0	1	1	0	**2 V_{DC}**
0	0	1	1	0	0	1	0	0	1	**1 V_{DC}**
0	0	1	1	0	0	0	0	1	1	**0**
0	0	1	1	0	0	0	1	1	0	**-1 V_{DC}**
0	1	1	0	0	0	1	0	0	1	**-2 V_{DC}**
0	1	1	0	0	0	0	0	1	1	**-3 V_{DC}**
0	1	1	0	0	0	0	1	1	0	**-4 V_{DC}**
0	0	0	1	1	0	1	0	0	1	**-5 V_{DC}**
0	0	0	1	1	0	0	0	1	1	**-6 V_{DC}**
0	0	0	1	1	0	0	1	1	0	**-7 V_{DC}**
0	1	0	0	1	0	1	0	0	1	**-8 V_{DC}**
0	1	0	0	1	0	0	0	1	1	**-9 V_{DC}**
0	1	0	0	1	0	0	1	1	0	**-10 V_{DC}**

other modes, current flows in one direction current path. Thus, $S_3 - S_4$ should be bidirectional switches and all the others should be unidirectional switches. The proposed asymmetrical source configuration for the main module is realized as $V_1 = V_{DC}$, $V_2 = 3V_{DC}$, and $V_3 = 6V_{DC}$.

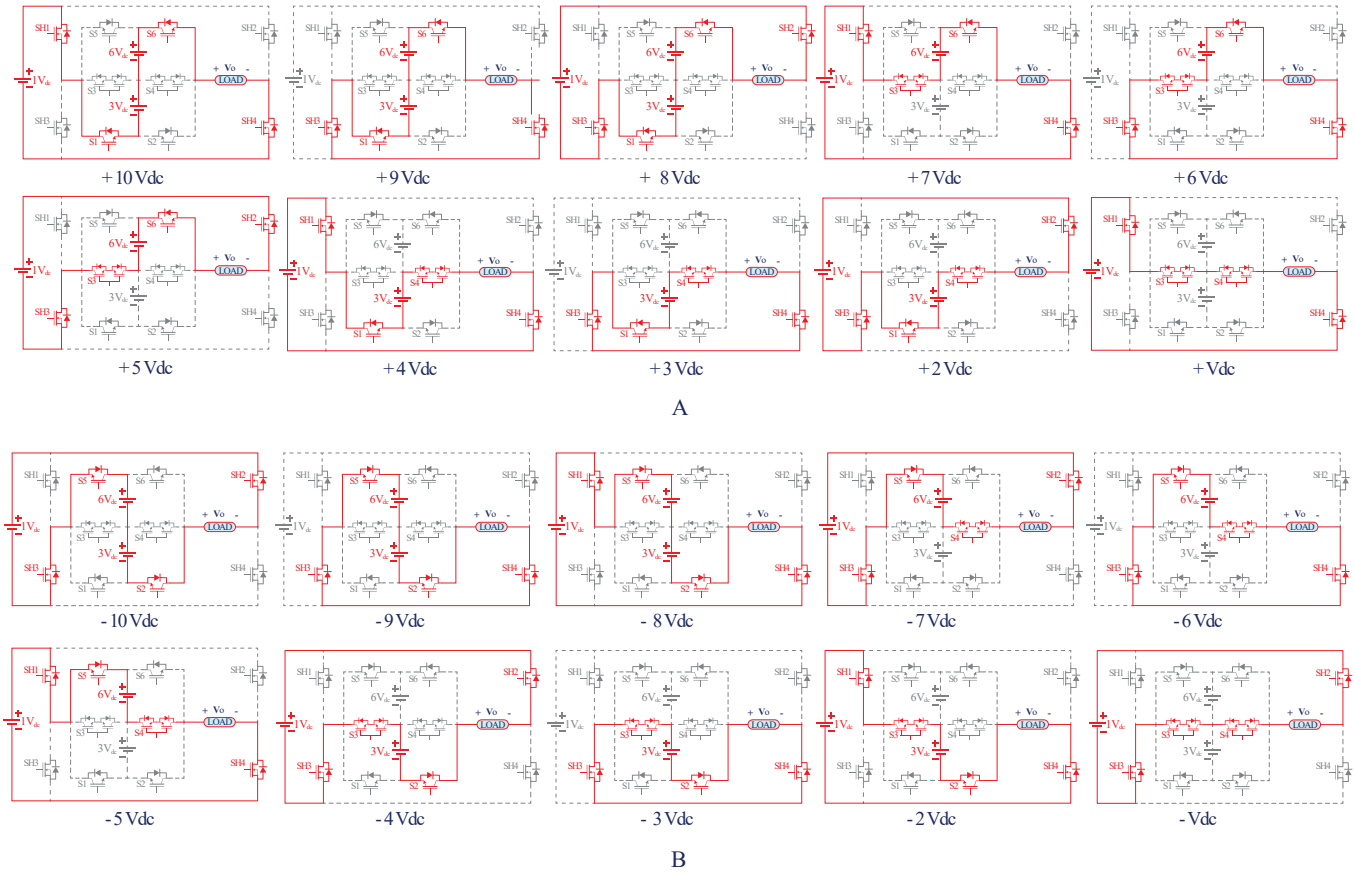


Figure 2 Different switching states of proposed module for (A) positive and (B) negative levels.

2.2 | Module Configuration

The switching states are defined in Table 1 and the circuit modes showing these states are presented in Figure 2. Figure 2A,B shows the modes of positive and negative voltage levels, respectively. The switches on the current path are ON, while all the others must be OFF. On the other hand, the switch pairs (S_{H1}, S_{H3}) and (S_{H2}, S_{H4}) must not be open at the same time, thus they operate in complementary mode.

Figure 3 exhibits one cycle of the output voltage waveform and the pulse signals of the switches. As seen in the figure, switches operate at different switching frequencies. Besides, it can be seen that the (S_{H1}, S_{H3}) and (S_{H2}, S_{H4}) switch pairs are triggered inversely. From the switching signals in Figure 3, it can be seen that switches S_5 and S_6 operate at the fundamental frequency, while the other switches operate at multiples of the fundamental frequency.

Total standing voltage (TSV) is expressed as the sum of the maximum voltages across each switch. Maximum voltage blocking of each switch for TSV calculation as,

$$\begin{aligned} V_{SH1} &= V_{SH2} = V_{SH3} = V_{SH4} = 1\,V_{DC} \\ V_{S1} &= V_{S2} = V_{S5} = V_{S6} \\ &= 3\,V_{DC} + 6\,V_{DC} = 9\,V_{DC} \\ V_{S3} &= V_{S4} = 6\,V_{DC} \end{aligned} \tag{1}$$

where V_{Si}, is the blocking voltage of the switches S_i respectively. Thus, TSV of the basic module is calculated as follows

$$\begin{aligned} TSV &= \sum_{k=1}^{4} V_{SHk} + \sum_{i=1}^{6} V_{Si} \\ &= 4.1V_{DC} + 4.9V_{DC} + 2.6V_{DC} = 52V_{DC} \end{aligned} \tag{2}$$

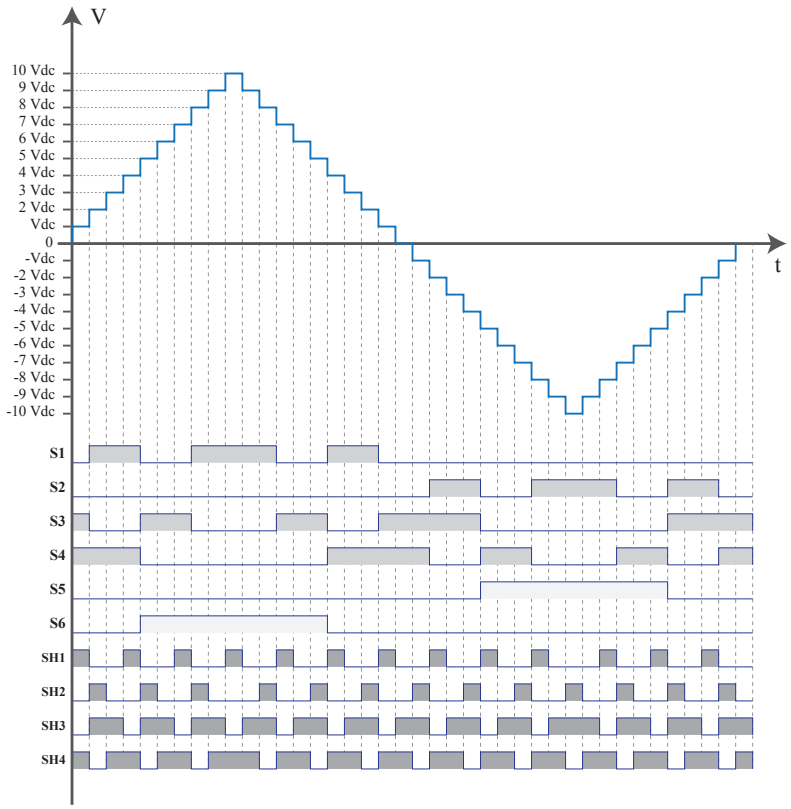


Figure 3 Switching pattern of the proposed module.

Figure 4 and Figure 5 depicts the voltage stress across the switches for each level. As can be seen, the blocking voltage of higher-frequency switches S_{H1}, S_{H2}, S_{H3}, S_{H4} is 1 V_{DC}, while the blocking voltage of lower-frequency switches S_1, S_2, S_5, S_6 is 9 V_{DC}, and S_3, S_4 is 6 V_{DC}. Note that some switches block different voltage amplitudes for different levels. However, the voltage stress of the respective switch will be the maximum blocking voltage. Besides, it can be seen from the graphs, the sum of the maximum blocking voltage of all switches will be 52 V_{DC}.

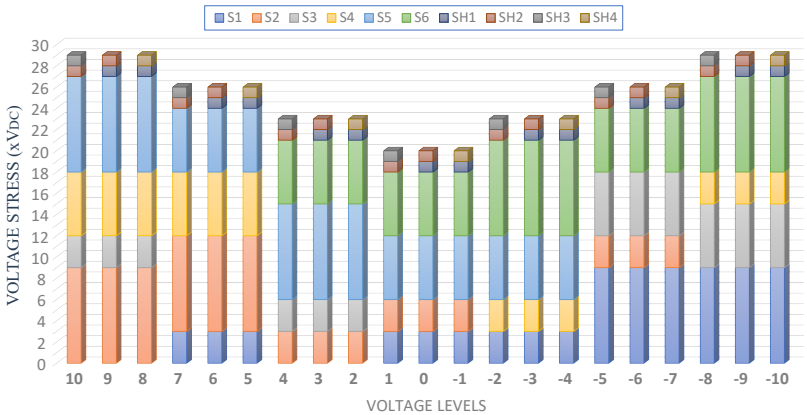


Figure 4 Voltage stress across to switches.

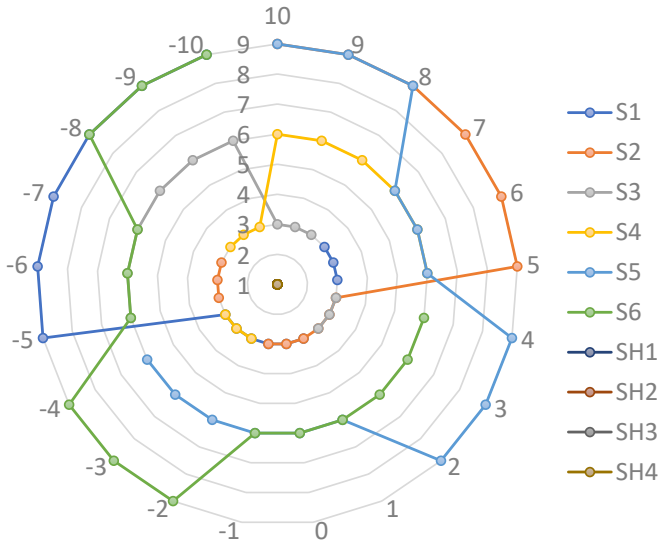


Figure 5 Voltage stress across to switches.

3 | EXTENSION TOPOLOGIES OF PROPOSED MLI

Figure 6 shows three options for extending the proposed topology. The first structure MODE-1 presented in Figure 6A has asymmetrical cascaded H-Bridges. Furthermore, the proposed first configuration with H-Bridge can extend all non-extendable topologies. The second one shown in Figure 6B is the classical symmetrical configuration. Figure 6C shows asymmetrical configuration method.

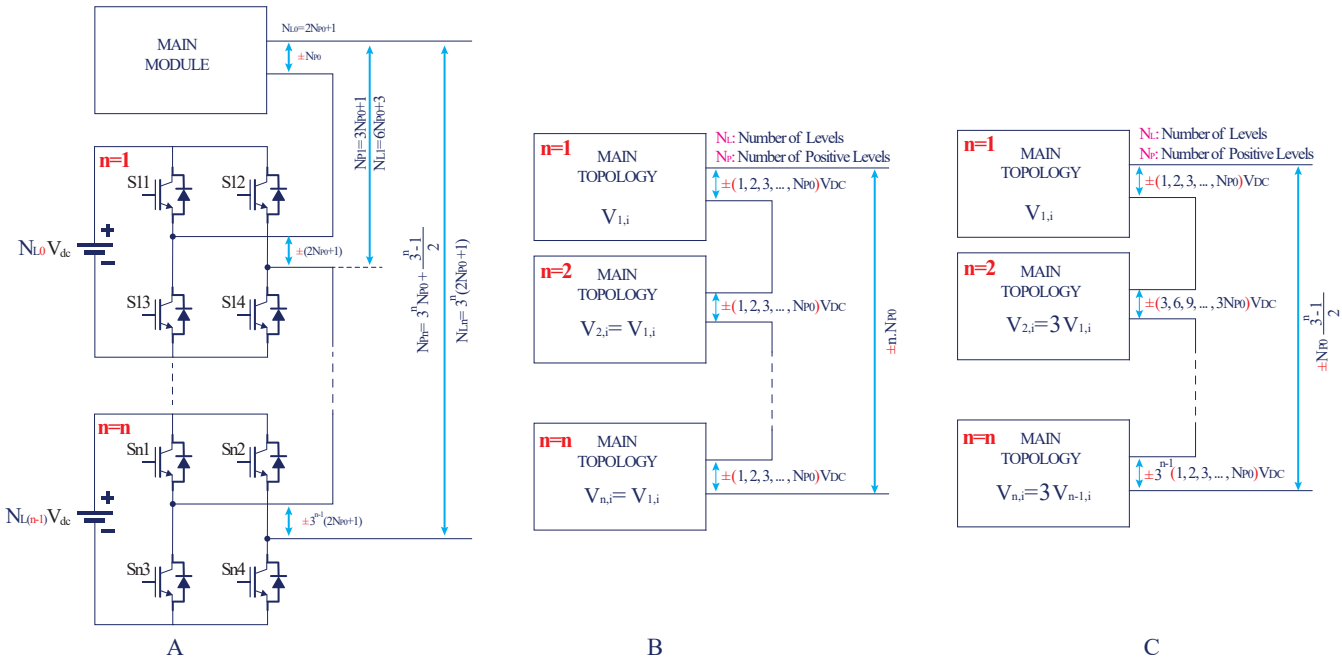


Figure 6 Proposed extension topologies (A) Cascaded with H-Bridge (Mode I), (B) Symmetrical Cascaded (Mode II), (C) Asymmetrical Cascaded (Mode III)

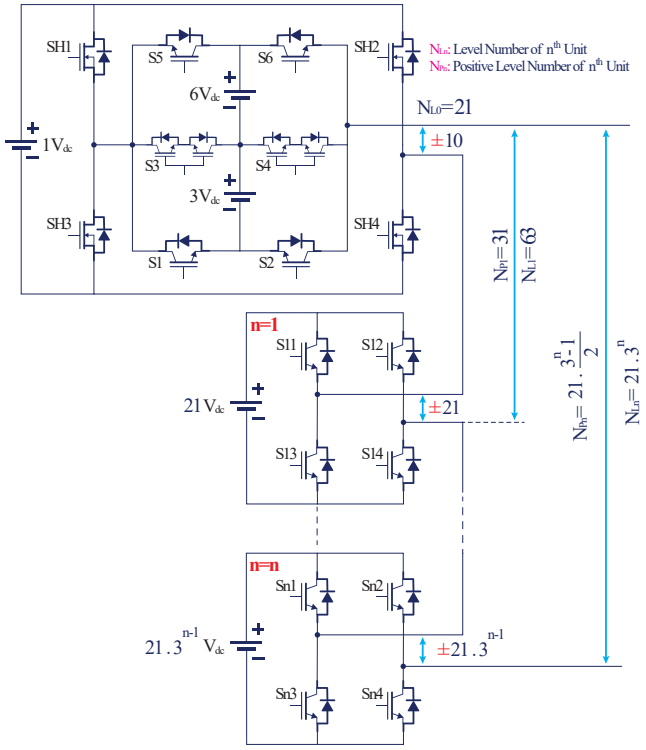


Figure 7 Main structure of first proposed extension topology (MODE I)

3.1 | Hybrid CHB extension topology (MODE-1)

In this approach, the proposed topology is extended by successive H-bridges containing independent DC sources. Figure 7 shows the main structure of the proposed extension structure with H-Bridge. The amplitude of the voltage source of each additional module is equal to the maximum voltage amplitude synthesized by the cascade structure up to the previous module. For example, the input voltage of the first H-bridge to be connected should be $21V_{DC}$, and the input voltage of the second H-bridge to be connected should be $63V_{DC}$.

For n number of module with such extension topology, the equations for the number of switches (N_{SW}), diodes (N_D), DC power supplies (N_{DC}), variety of dc power supplies (N_{VR}), gate driver (N_{GD}), and the number of levels (N_L) are given as:

$$\begin{aligned} N_L &= 21.3^n \\ N_{SW} &= 4n + 12 \\ N_{DC} &= n + 3 \\ N_{VR} &= n + 3 \\ N_{GD} &= 4n + 10 \end{aligned} \tag{3}$$

Calculation of TSV will be as follows
Voltage stress of switches on H-Bridges

$$\begin{aligned} V_{11} &= V_{12} = V_{13} = V_{14} = 21\,V_{DC} \\ V_{21} &= V_{22} = V_{23} = V_{24} = 21.3\,V_{DC} \\ V_{31} &= V_{32} = V_{33} = V_{34} = 21.3^2\,V_{DC} \\ &\vdots \\ V_{n1} &= V_{n2} = V_{n3} = V_{n4} = 21.3^{n-1}\,V_{DC} \end{aligned} \tag{4}$$

$$21\left(1 + 3 + 3^2 + \cdots + 3^{n-1}\right) = 21.\frac{3^n - 1}{2} \tag{5}$$

$$TSV_1 = 4.\left(21.\frac{3^n - 1}{2}\right) = 42.(3^n - 1) \tag{6}$$

TSV of the main module is calculated above in Eq. (2)

$$TSV_2 = 52\,V_{DC} \tag{7}$$

$$\begin{aligned} TSV &= TSV_1 + TSV_2 = 42.(3^n - 1) + 52 \\ TSV &= 42.3^n + 10 \end{aligned} \tag{8}$$

3.2 | Cascaded extension topologies (Symmetrical and Asymmetrical mode)

Two cascaded extension topologies with proposed 21 level MLI consists of a cascade serial connection of the main module with asymmetrical and symmetrical dc sources respectively. Figure 8 shows the cascade connection of the proposed 21 level MLI.

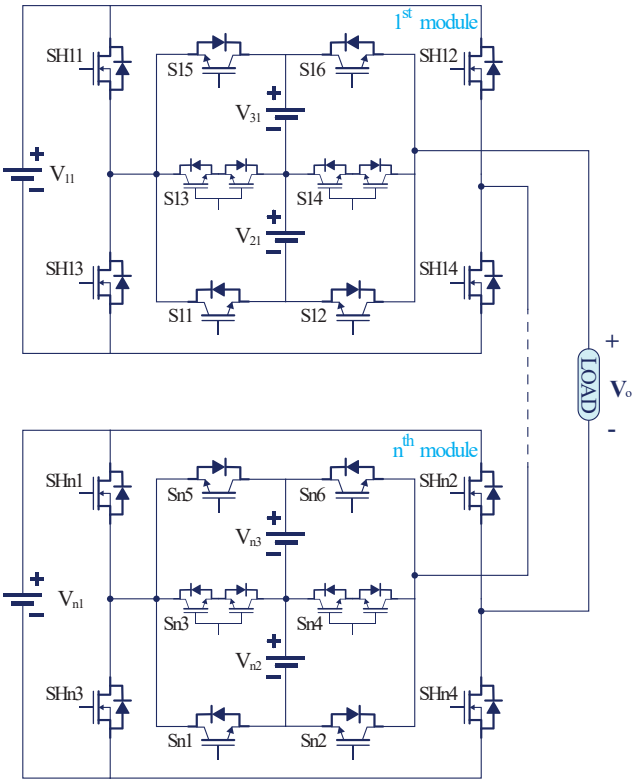


Figure 8 Cascaded connection of proposed 21 level MLI

3.2.1 | Symmetrical extension topology (MODE-2)

Symmetric source configuration does not mean that the magnitude of the source voltages in the main module is equal, it means that the magnitude of the source voltages in the same subindex in each module is symmetrical. In other words, the amplitudes of the voltage sources in each module will be V_{n1}= 1 V_{DC}, V_{n2}= 3 V_{DC}, and V_{n3}= 6 V_{DC}, respectively. For the n number of

modules, the equations of the cascade expansion structure with the symmetrical configuration shown in Figure 8 are given as

$$\begin{aligned} N_L &= 21n \\ N_{SW} &= 12n \\ N_{DC} &= 3n \\ N_{VR} &= 3 \\ N_{GD} &= 10n \end{aligned} \tag{9}$$

Since the maximum voltage stresses appearing on the switches are equal for the same numbered switches in each module, the TSV of all modules will be equal. Sum of the TSVs of all submodules are

$$TSV = \sum_{1}^{n} TSV_n = \sum_{1}^{n} 52\ V_{DC} = 52n\ V_{DC} \tag{10}$$

3.2.2 | Asymmetrical extension topology (MODE-3)

In the expansion structure shown in Figure 8, dc sources with the same subindex are configured with Trinary source configuration in order to synthesize higher number of levels at the output voltage waveform. As a result of Trinary source configuration, magnitudes of dc sources will be as seen in Eq. (11).

$$\begin{array}{lll} V_{11} = 1\ V_{DC} & V_{12} = 3\ V_{DC} & V_{13} = 6\ V_{DC} \\ V_{21} = 3\ V_{DC} & V_{22} = 9\ V_{DC} & V_{23} = 18\ V_{DC} \\ V_{31} = 9\ V_{DC} & V_{32} = 27\ V_{DC} & V_{33} = 54\ V_{DC} \\ \vdots & \vdots & \vdots \\ V_{n1} = 3^{n-1}\ V_{DC} & V_{n2} = 3^{n}\ V_{DC} & V_{n3} = 2.3^{n}\ V_{DC} \end{array} \tag{11}$$

For the n number of modules, the equations of the cascade expansion structure with the Asymmetrical configuration are given as

$$\left.\begin{array}{rl} N_L &= 10.3^n - 9 \\ N_{SW} &= 12n \\ N_{DC} &= 3n \\ N_{VR} &= 2n+1 \\ N_{GD} &= 10n \end{array}\right\} \tag{12}$$

Since the amplitude of DC sources with the same subindex in each module is three times of the previous module, the TSV of the relevant module will be three times of the previous module. TSV of the nth module will be as follow

$$\begin{aligned} TSV_1 &= 52\,V_{DC} \\ TSV_2 &= 52.3\,V_{DC} \\ TSV_3 &= 52.3^2\,V_{DC} \\ &\vdots \\ TSV_n &= 52.3^2 V_{DC} \end{aligned} \tag{13}$$

The TSV sum of all modules will be as

$$\begin{aligned} TSV &= \sum_{i=1}^{n} TSV_i = 52 + 52.3 + 52.3^2 + \cdots + 52.3^{n-1} \\ TSV &= 52\left(1 + 3 + 3^2 + \cdots + 3^{n-1}\right) = 52\tfrac{3^n-1}{2} \\ TSV &= 26\,(3^n - 1) \end{aligned} \tag{14}$$

For calculation of the number of DC source variation, let we write all DC sources for n modules

$$\begin{bmatrix} 1 & 3 & 6 \\ 3 & 9 & 18 \\ 9 & 27 & 54 \\ \vdots & \vdots & \vdots \\ 3^{n-1} & 3^n & 2.3^n \end{bmatrix} \rightarrow\ 1, 3, 9, \cdots, 3^n, 2.3, 2.3^2, \cdots, 2.3^n \tag{15}$$

We have 2n+1 unique DC sources from Eq.(15). The number of DC source variations for n modules is

$$N_{VR} = 2n + 1 \tag{16}$$

4 | COMPARATIVE STUDY

Table 2 Comparison of the Proposed Modes with Some Extendable MLI Topologies

Topology	N_{SW}	N_D	N_{DC}	N_{VR}	N_{GD}	TSV (xV_{DC})
NPC (Conventional)	$2(N_L-1)$	N_L+1	$(N_L-1)/2$	1	$2(N_L-1)$	$2(N_L-1)$
FC (Conventional)	$2(N_L-1)$	$2(N_L-1)$	N_L-2	1	$2(N_L-1)$	$2(N_L-1)$
CHB (Conventional)	$2(N_L-1)$	$2(N_L-1)$	$(N_L-1)/2$	1	$2(N_L-1)$	$2(N_L-1)$
CHB (Binary)	$4[\log_2(N_L+1)-1]$	$4[\log_2(N_L+1)-1]$	$\log_2(N_L+1)-1$	$\log_2(N_L+1)-1$	$4[\log_2(N_L+1)-1]$	$2(N_L-1)$
MLDLC [23]	N_L+3	N_L+3	$(N_L-1)/2$	1	N_L+3	$3(N_L-1)$
ST-Type [24]	$12\log_{17} N_L$	$12\log_{17} N_L$	$4\log_{17} N_L$	$2\log_{17} N_L$	$9\log_{17} N_L$	$2{,}5(N_L-1)$
K-Type [25]	$14\log_{13} N_L$	$14\log_{13} N_L$	$4\log_{13} N_L$	$2\log_{13} N_L$	$11\log_{13} N_L$	$8(N_L+10)/3$
SD-MLI [2]	$3\log_6(N_L+0.5)+4$	$6\log_6(N_L+0.5)+4$	$3\log_6(N_L+0.5)$	$2\log_6(N_L+0.5)$	$3\log_6(N_L+0.5)+4$	$3\log_6(N_L+0.5)+4$
MODE-I (Hybrid)	$4\log_3(N_L/21)+12$	$4\log_3(N_L/21)+12$	$\log_3(N_L/21)+3$	$\log_3(N_L/21)+3$	$4\log_3(N_L/21)+10$	$2N_L+10$
MODE-II (Symmetric)	$4N_L/7$	$N_L/7$	$N_L/7$	3	$10N_L/21$	$52\,N_L/21$
MODE-III (Asymmetric)	$12\log_3((N_L+9)/10)$	$12\log_3((N_L+9)/10)$	$3\log_3((N_L+9)/10)$	$2\log_3((N_L+9)/10)+1$	$10\log_3((N_L+9)/10)$	$2\log_3((N_L+9)/10)+1$

The proposed topology has been compared with traditional and recently proposed MLI topologies based on reduced switch count. The variation of the number of components of symmetric topologies against the number of levels at the output is generally linear, while that of asymmetric topologies is logarithmic. Thus, the symmetric extension topology of the proposed module (MODE II) has been compared with the symmetric topologies (NPC[5], FC[6], CHB[7], MLDLC[23]), while the asymmetric extension topologies (MODE I-III) have been compared with the asymmetric topologies (CHB Binary[8], ST-Type[24], K-Type[25], SD-MLI[2]) in the literature. The comparative study has been made for the number of switches (N_{SW}), diodes (N_D), DC power supplies (N_{DC}), variety of DC power supplies (N_{VR}), gate drivers (N_{GD}), and the number of levels (N_L) as shown in Table 2. Figure 9 shows the variation of number of levels in the number of required power components of all symmetric and asymmetric MLIs. Symmetric and asymmetric topologies are compared with themselves, and the results of the comparison are shown in the same figures. Therefore, the curves of symmetric topologies are indicated with dashed lines and asymmetric topologies with straight lines. The dashed lines in Figure 9A show that the proposed MODE II topology needs fewer power switches. On the other hand, MODE I is one of the topologies that require minimum number of switches among asymmetrical structures as seen in the figure. Since curves of the CHB Binary, MODE 1, and SD-MLI topologies are closest, the zoomed version of the relevant region is placed under the figure. In Figure 9B,C,D,E , MODE II and MODE I offer better results in all other symmetric and asymmetric comparisons, respectively. Figure 9F shows that the TSV is lower than many other topologies.

5 | NEAREST LEVEL CONTROL

There are several modulation techniques to generate the switching pulses of multilevel inverters. Modulation techniques in multilevel inverters based on switching frequency are divided into two main categories, these are fundamental switching frequency techniques and high switching frequency techniques. Especially in high-power applications, fundamental switching frequency techniques are frequently used. Fundamental frequency modulation techniques that are optimal switching techniques,

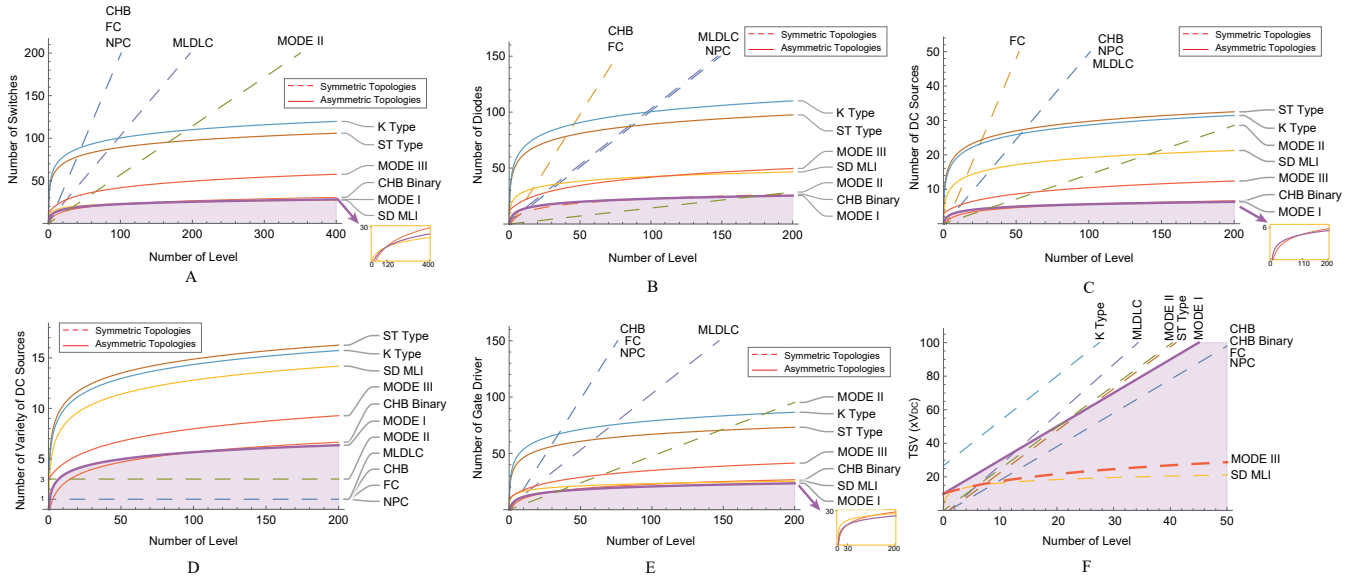


Figure 9 Comparison studies, Number of levels against (A) number of switches, (B) number of diodes, (C) number of DC sources, (D) number of variety of DC sources, (E) number of gate drivers and (F) total standing voltage

selective harmonic elimination (SHE)[26], and nearest level control methods[27,28] are frequently preferred in high-power applications. SHE method mitigates lower-order harmonics notably thus reducing filter size and complexity but has nonlinear transcendental equations that are used to eliminate lower-order harmonics. The main problem associated with SHE is solving transcendental equations due to their complexity. The nearest level control technique is generally used to eliminate the drawbacks of SHE. In this paper, the NLC modulation method has been used for trigger control of the proposed multilevel inverter, in which the switching losses and lower-order harmonics are reduced. Figure 10 shows the working principle and control diagram of the NLC method. The reference voltage (Vref) is sampled at one point and then rounded to the nearest voltage level (VaN) as shown in Figure 10A. Figure 10B depicts the schematic representation of NLC implementation.

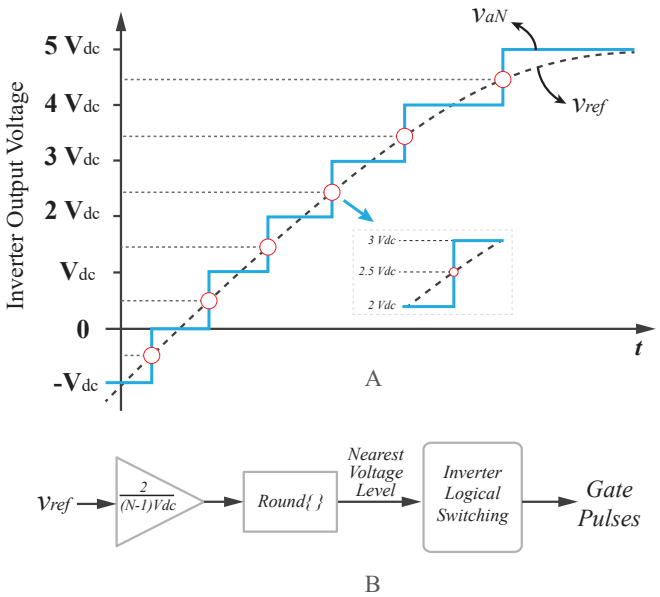


Figure 10 Nearest level control modulation (A) sampled reference signal, (A) implementation of NLC.

6 | RESULTS AND DISCUSSION

A laboratory prototype of the main module has been performed to verify the performance of the proposed topology. Simulation and experimental studies have been carried out on this prototype. The simulation and experimental study have been discussed in this section and the simulation results have been verified with the experimental results.

6.1 | Simulation Results

The proposed basic unit has been simulated with the NLC control method using MATLAB/Simulink software. For the simulation study, DC voltage sources are arranged as V_1=10 V, V_2=30 V and V_3=60 V. The simulation has been performed with purely resistive ($R_{Load} = 100\Omega$) and resistive-inductive loads ($RL_{Load} = 100\Omega + 50mH$, $RL_{Load} = 100\Omega + 200mH$). Figure 12A,B,C shows transient and steady state responses of the voltage and current with different load conditions, modulation indexes, and frequencies respectively. The change of load type from purely resistive R_{Load} to resistive-inductive RL_{Load} loads has been depicted in Figure 12A. All Y-axises in Figure 12 are scaled differently on the right and left sides to show both voltage and current waveform in one figure. The harmonic spectrum of the output voltage and current on R_L load is depicted in Figure 11. The THD of voltage and current waveforms are evaluated 3.90% and 0.22%, respectively. It is observed that the magnitudes of harmonic orders in the current waveform decrease compared to the voltage waveform due to the series-connected inductive load.

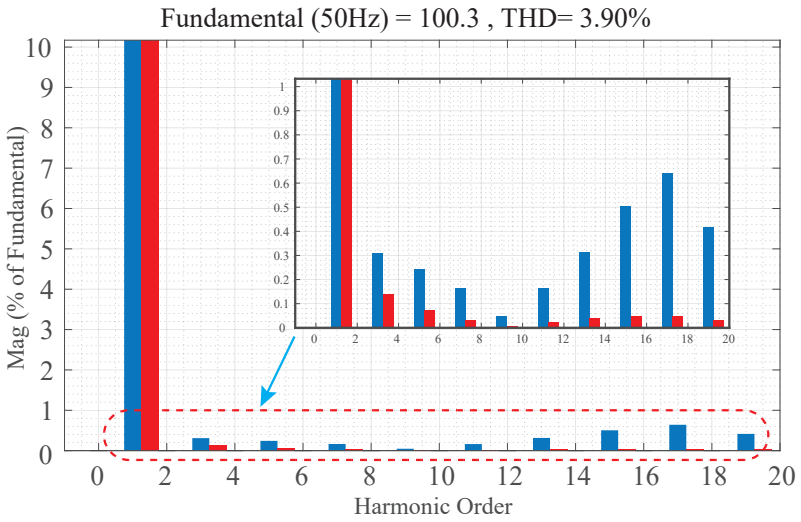


Figure 11 Harmonic analysis of the output voltage and current

6.2 | Experimental Study

A laboratory prototype has been developed to verify the performance of the proposed topology as shown in Figure 13. For the experimental study, step voltages of the three dc sources are set as Vdc=10V. Genesys 2 FPGA board has been used to generate the switching pulses. The output waveforms of the voltage and current on the series-connected purely resistive load ($R_{Load} = 100\Omega$) are shown in Figure 14. In Figure 15 the circuit has been tested under different resistive-inductive load conditions and the output waveforms are presented. Furthermore, It has been tested at different modulation indexes and transient responses are also shown in Figure 16. Finally, 50 Hz and 100 Hz output waveforms are presented in Figure 17 to demonstrate their operability at higher frequencies. Experimental study shows that proposed MLIs synthesize all levels and proves that experimental results and simulation results are confirmed.

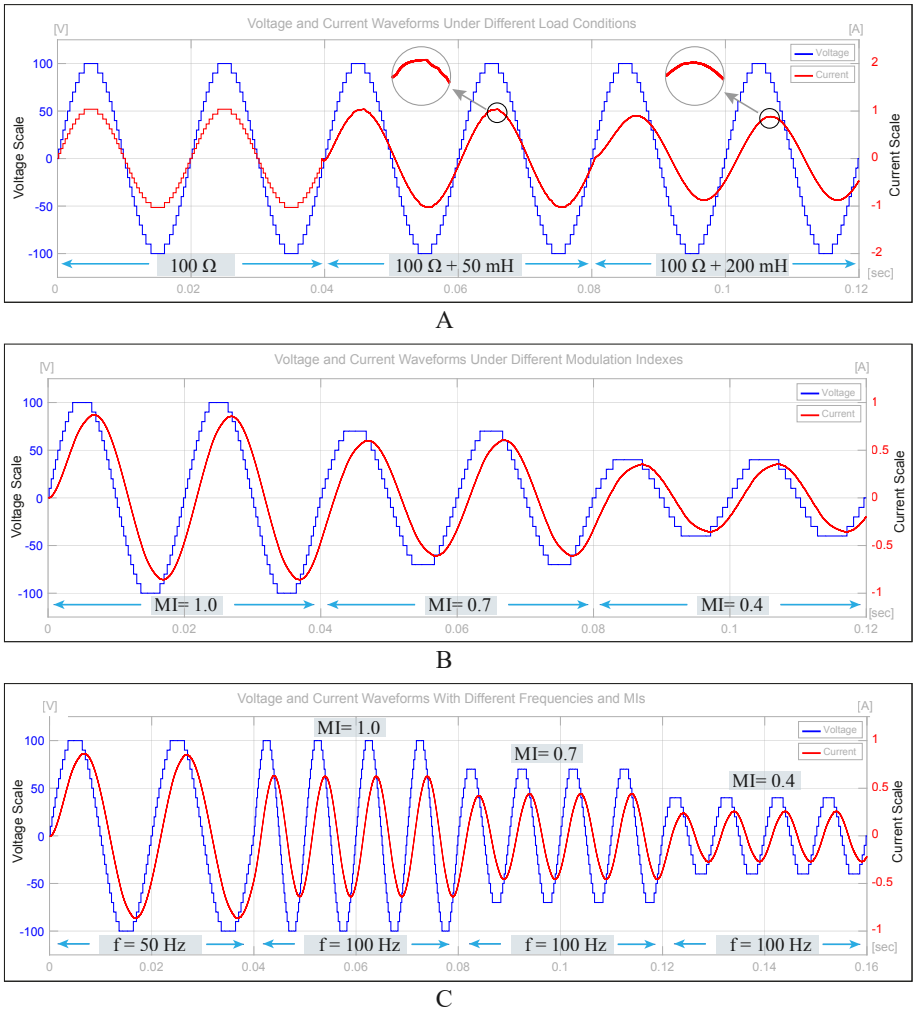


Figure 12 Voltage and Current waveform under different states (A) Load Condition, (B) Modulation Index, (C) Frequency

7 | CONCLUSION

This paper introduced a new MLI with an asymmetric source configuration. The proposed topology consists of two main parts: high frequency H-Bridge circuit fed by one source and switched sources unit. The proposed MLI synthesizes 21 levels with the minimum number of power switches. Experimental and simulation studies have been carried out and the results prove that the proposed module generates higher output voltage levels with fewer components such as 3 DC sources and 10 switches. Furthermore, for the accuracy of the proposed topology, the simulation, and experimental studies have been performed under different load conditions, MI, and frequencies and results are compared. The other significant result is that the THD obtained 3.99% which meets the harmonics standard (IEE519). Since the topology is 21-level, pure sine output current can be obtained with a low value filter. However, a high value filter is used to show that the topology can operate at low power factors. Also the MLI supports variable MI and frequency. This shows that the proposed topology is suitable for use in electric vehicle and other motor applications. In order to produce higher levels in the output voltage waveform, the proposed structure is extended by three different methods, and compared with commonly used topologies in the literature. Comparison results show that the proposed topology has the reasonable performance compared to its counterparts in the literature.

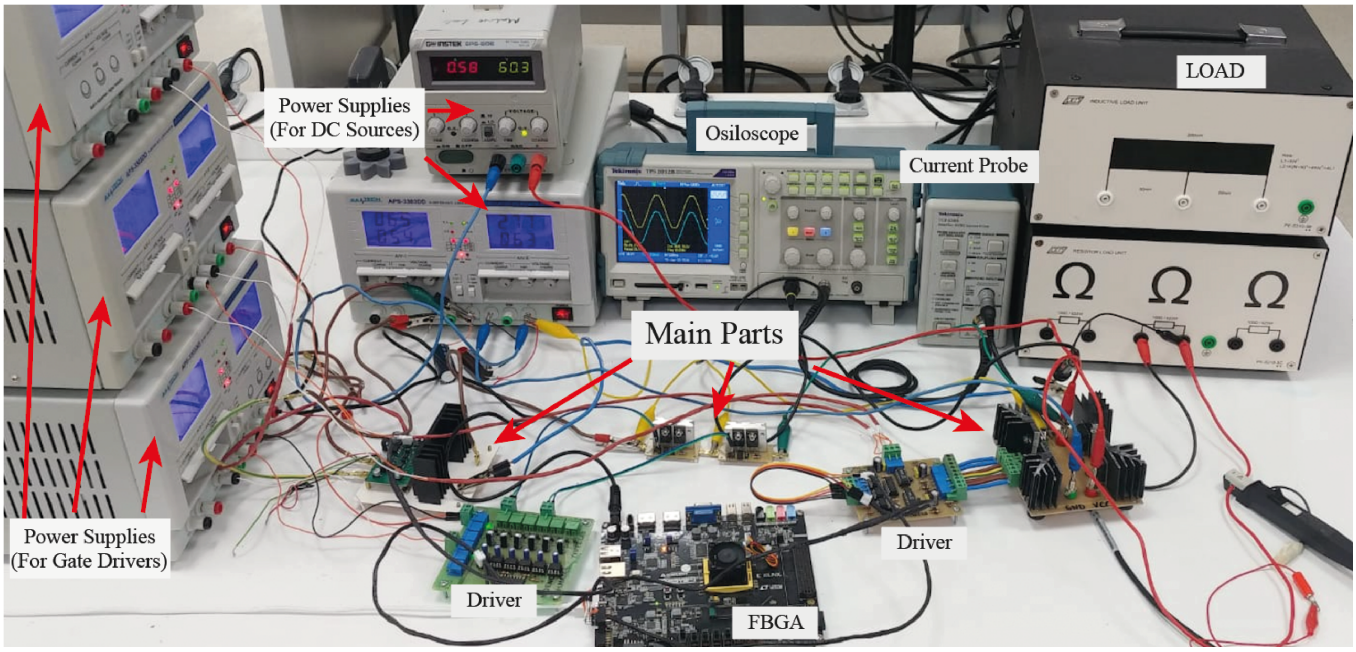
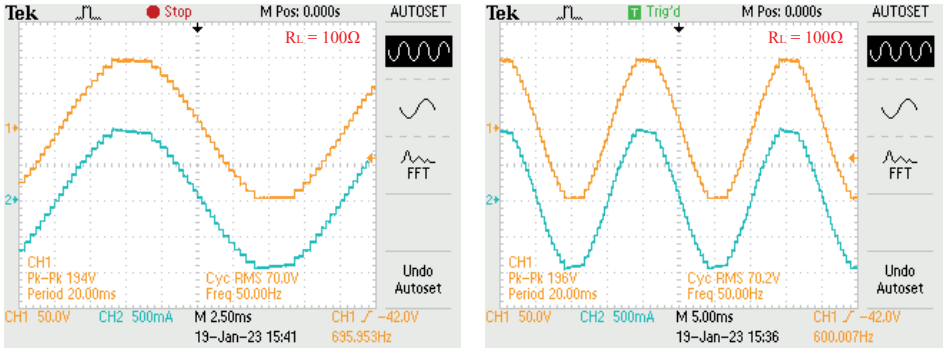


Figure 13 Experimental setup of proposed MLI



A B

Figure 14 Experimental results. (A,B) voltage and current waveform

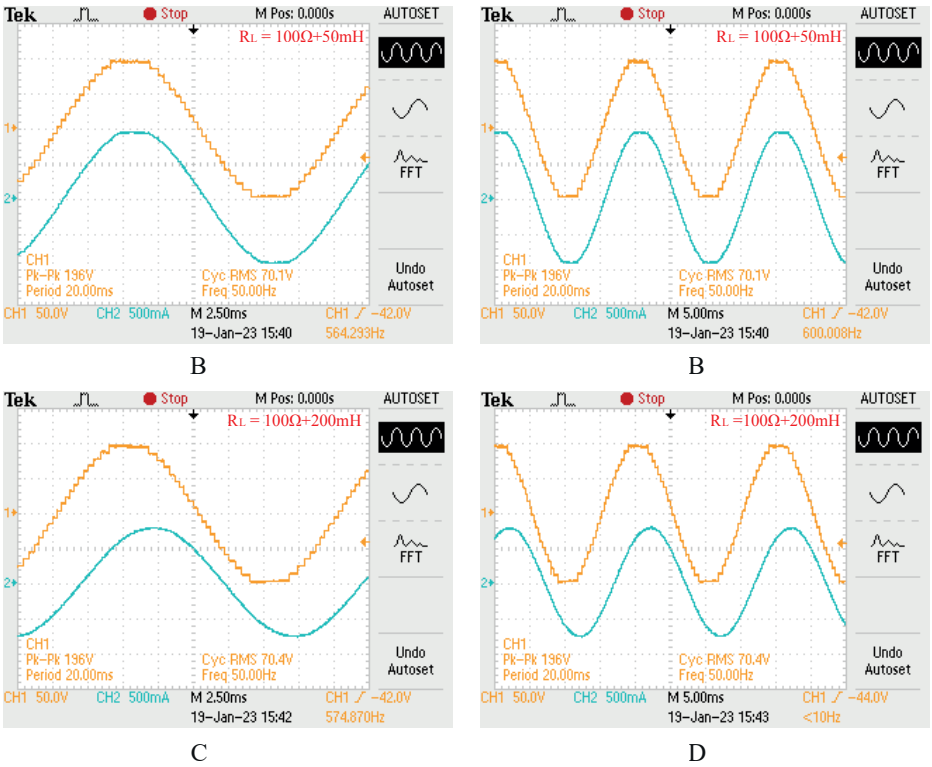


Figure 15 Experimental results. Voltage and current waveform under different load conditions (A,B) $RL_{Load} = 100\Omega + 50mH$ (C,D) $RL_{Load} = 100\Omega + 200mH$

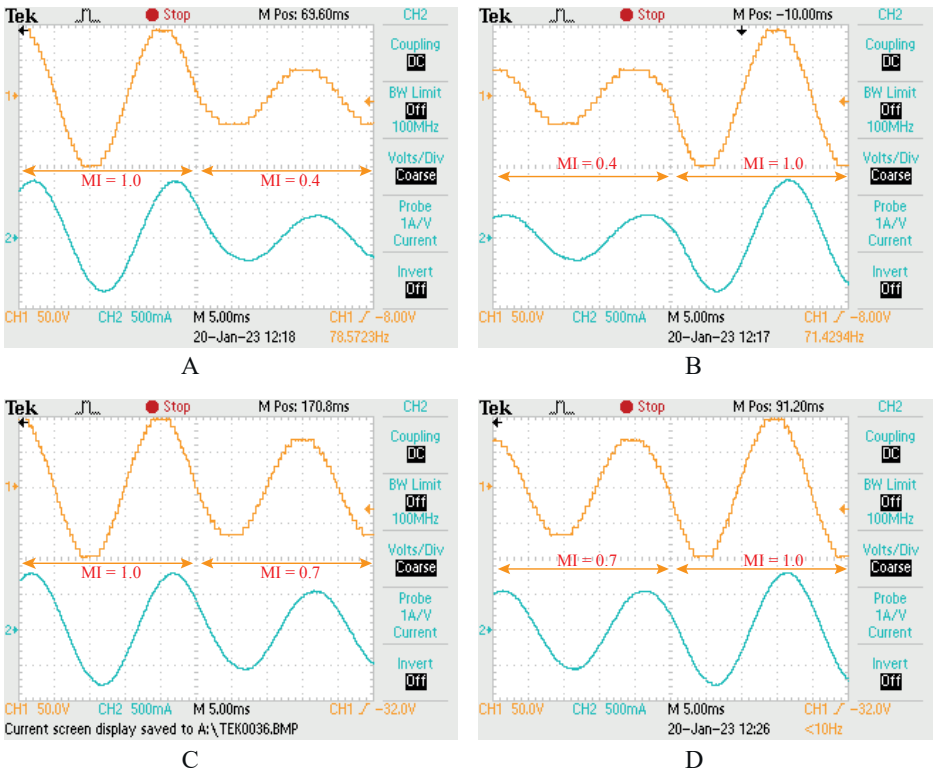
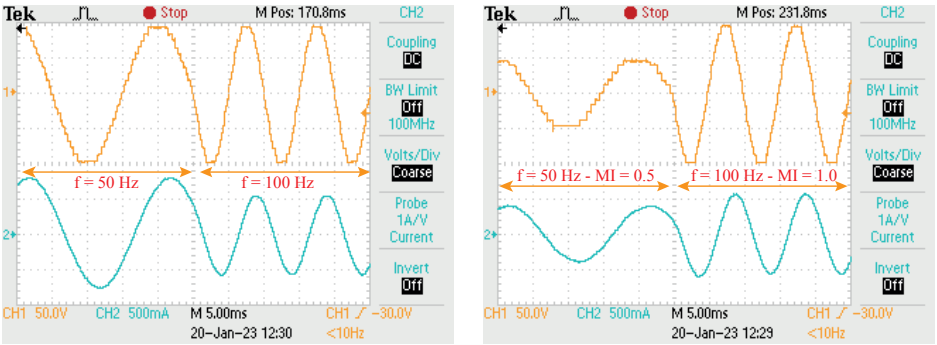


Figure 16 Experimental results after changing MI values from (A) 1.0 to 0.4 (B) 0.4 to 1.0. (C) 1.0 to 0.7 and (D) 0.7 to 1.0



A B

Figure 17 Experimental results after changing together MI and frequency values from (A) MI:1.0 to 1.0 and f:50 Hz to 100 Hz (B) MI:0.5 to 1.0 to f:50 Hz to 100 Hz

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