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A Sub-nW 100 ppm/°C Self-Biased Voltage Reference Circuit for IOT Applications.

TARANVEER KAUR[1] and Arvind kumar[1]

[1]Panjab University

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Abstract

A sub-nW, self-biased voltage reference circuit is developed to provide bias signals for use in Internet-of-Things (IOT) applications, taking use of the sub-threshold region operation MOSFETs. Circuit is evaluated by simulation with 180nm SCL's CMOS device parameters and 1.8 V voltage supply and from temperature -40@C to 125@C. Simulation shows that a temperature sensitivity of designed voltage reference is less than 100 ppm/°C. The size of the proposed design without IO pads is 30 µm × 30 µm and consumes power less than 50 nW.

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Introduction: References, voltage or current are essential parts of various systems. They produce constant output voltages for required application-based temperature range and act as process, voltage, and temperature insensitive references. Critical for developing energy-constrained systems, including the biomedical devices and self-powered wearable electronic gadgets. To reduce idle power consumption and extend operational life when working with restricted source energy, these systems attract the mixed-signal ICs to a nano-watt or pico-watt voltage reference [1][2]. Additionally, the voltage reference should be able to function at low supply voltages [3][4] like 1.2V, 0.5 V or even lower because the supply voltages of ICs are repeatedly decreasing due to process scaling. The demand for low-power analog mixed signal (AMS) circuits has rapidly increased in the present period due to the limited size and capacity of battery devices. Voltage reference circuits are essential for providing a precise and stable DC bias in AMS circuits like ADC/DAC comparators, operational amplifiers, PLLs, etc. in any kind of environment. Due to scaling of voltage and power, there has been a significant challenge in the design of voltage reference circuits. Voltage references are an important block of these AMS circuits and overall performance heavily depends on the performance of the voltage reference circuits. Many analog circuits find the use of temperature independent reference voltages or currents indispensable. Since most process parameters are also affected by temperature, a voltage reference that is temperature-independent is also less process-independent. The two main forms of VRs are BJT based band-gap voltage references and using subthreshold property of CMOS based voltage references. The conventional structure of bandgap-based voltage reference (BGR) [5] provides a constant voltage depending on the current-V_{BE} properties of the diode [6]. The CMOS transistors are used by CVR to create a stable reference voltage. Because resistors are required in traditional BGR designs, BGR rarely achieves low power consumption, which has an impact on the operation of ultra-low-power applications like Internet of Things devices. The low temperature sensitivity reference voltages could not be produced by the conventional band-gap voltage reference technique, which mostly consists of lateral PNP transistors [7], at a supply level below 1V without the use of additional circuits. Low power reference voltages and currents are also frequently produced by MOSFETs working in the sub-threshold region. Basic concept of the temperature independent voltage reference generation is adding with proper weighting of two quantities having opposite temperature dependencies, the output has zero temperature sensitivity [8]. If we add negative TC voltage VCTAT and positive TC voltage VPTAT with weight α and β such that.

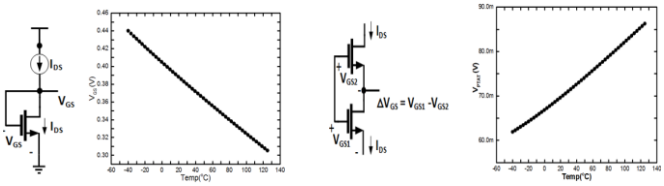
$$\alpha \frac{\partial V_{CTAT}}{\partial T} + \beta \frac{\partial V_{PTAT}}{\partial T} = 0 \qquad (1)$$

In this work, designed a low power voltage reference circuit for across a temperature range from -40˚C to 125˚C using subthreshold property of MOS.

Operating Principle: In sub-threshold region, all currents must be created by diffusion because there are no moderately or strongly inverted portions of the channel and the electric field has no horizontal component. [9]. Assuming long channel length, if $V_{DS}>4\Phi_T$, the expression for drain current then simplifies to

$$I_{DS} = I_S \exp\left(\frac{V_{GS} - V_{TH}}{n\Phi_T}\right) \qquad (2)$$

$$I_S = 2n\mu C_{ox} \frac{W}{L} {\Phi_T}^2 \qquad (3)$$



a b

Fig. 1 (a) *VGS versus Temperature;* (b) *VPTAT versus Temperature*

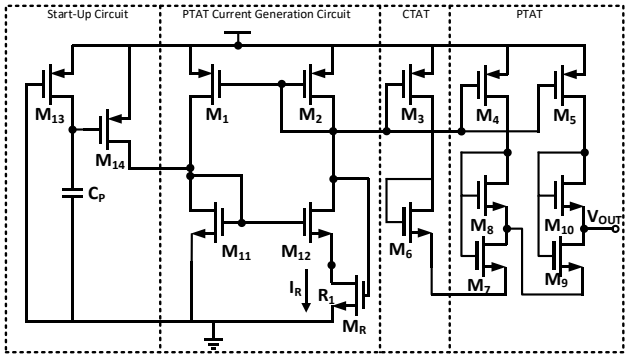


Fig. 2 circuit diagram of proposed work

The configuration of Fig.1, NMOS transistor simulated using a 180nm standard CMOS process parameters at 1V power supply. Transistor was biased with 100nA current, generates CTAT and PTAT voltages, as

$$V_{GS} = n\Phi_T \, ln\left(\frac{I_D}{I_S}\right) + V_{TH} \qquad (4)$$

$$V_{TH}(T) = V_{TH}(T_0) + \mathrm{k}(\mathrm{T} - T_0) \qquad (5)$$

$$\triangle V_{GS} = V_{GS1} - V_{GS2} = V_{DS1} = n\Phi_T \ln\left[\frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_1} \frac{I_{DS1}}{I_{DS2}}\right] + (V_{TH1} - V_{TH2}) \qquad (6)$$

Where n is the sub-threshold slope factor which is in modern CMOS processes ranges between 1.3 to 1.5, V_{DS} is drain-source voltage, V_{TH} is threshold voltage, V_{GS} is gate-source voltage, Φ_T is thermal potential, T represent room temperature in Kelvin [300K], k (Boltzmann constant), q is charge of electron, for a given small drain current $V_{GS} \approx V_{TH}$. The size ratio of transistor $(W/L)_2/(W/L)_1$ should be higher than 20 [10] to ensure that M1 is working in saturation region. It should be noted that M1 and M2 must both be operating in weak inversion.

Circuit description of proposed work: The low power voltage reference circuit is shown in Fig.2, it has four main parts. M13, M14, Cp forms Start-up circuit to avoid zero bias condition and does not affect the final output voltage. MR is working in deep triode region and works as resistor R1, and its value can be chosen as

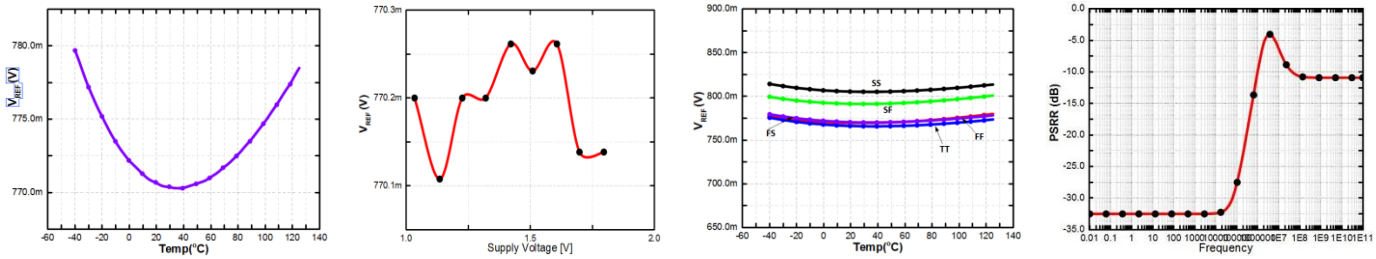
$$R_1 = \frac{L}{\mu C_{ox} W (V_{GS} - V_{TH})} \qquad (7)$$

M6 to M12 transistors operated in subthreshold region. M1, M2, M11, M12, R1 forms PTAT current generation circuit. Considering that $(W/L)_1 = (W/L)_2 = (W/L)_3$, the bias current (from Fig.2) is given by:

$$I_{BIAS} = \frac{(V_{GS1} - V_{GS2})}{R_1} \qquad (8)$$

For this proposed circuit, we choose IBIAS equal to ~ 357nA and R1 is equivalent to around 100 KΩ. M3 mirrors the PTAT current into diode connected M6 and generates CTAT voltage. M7, M8, M9, M10 forms PTAT generation circuits and M4, M5 mirrors the PTAT current into PTAT. VREF is a sum of CTAT voltage and a properly scaled PTAT voltage. The output voltage of the circuit is given by:

$$V_{REF} = V_{D14} + V_{DS7} + V_{DS9} \qquad (9)$$



3(a) Temperature dependence of Voltage reference (b) Vref function of supply voltage (C) Vref with different process corners (d)PSRR

The current through M4, M5 and M6 are respectively: (S4/S2) *IBIAS, (S5/S2) *IBIAS and (S6/S2) *IBIAS, S represents $\left(\frac{W}{L}\right)$. If neglect the body effect then,

$$V_{REF} = V_{D14} + (V_{GS7} - V_{GS8}) + (V_{GS9} - V_{GS10}) \quad (10)$$

$$V_{REF} = V_{D14} + n\Phi_T \ln\left[\frac{S_8}{S_7}\frac{I_{DS7}}{I_{DS8}}\right] + n\Phi_T \ln\left[\frac{S_{10}}{S_9}\frac{I_{DS9}}{I_{DS10}}\right] \quad (11)$$

$$I_{DS9} = I_{DS10} + \frac{S_6}{S_2} I_{BIAS} \quad (12)$$

$$V_{REF} = V_{D14} + n\Phi_T \ln\left[\frac{(S_4 + S_5 + S_6)(S_5 + S_6)S_8 S_{10}}{S_4 S_5 S_7 S_9}\right] + n\Phi_T \ln\left[\frac{S_8}{S_7}\frac{S_{10}}{S_9}\left(\frac{S_4 + S_5 + S_6}{S_2}\right)\frac{S_2}{S_4}\left(\frac{S_5 + S_6}{S_2}\right)\frac{S_2}{S_5}\right] \quad (13)$$

From (11) With the right device dimensions, slope of CTAT and PTAT can matched and (δVREF/ δT) = 0 can generate.

Design and Verification Result: Schematic and layout of the circuit done using Cadence Virtuoso software. Schematic of the sub-threshold based low power voltage reference circuit is shown in fig.2, and layout of the voltage reference has been done using 4-metal 180nm SCL's CMOS process and shown in fig.4. The die size of device is 30 µm × 30 µm. To verify the circuit behaviour, and to confirm the operation of sub-threshold MOS based voltage reference circuit, all simulations were performed using Synopsys H-spice Simulator using a set of standard 180nm CMOS process parameters. At typical process corner, room temperature and 1.8V voltage supply and circuit generates 770mV. Figure.3(a) shows a temperature stability results. Simulation performed from −40˚C to 125˚C temperature, and it achieves a temperature sensitivity of 100 ppm/°C in complete temperature range. To verify supply voltage stability in simulation, supply voltage varies from 1V to 1.8V and results is shown in figure.3(b). Reference voltage is varying approximately only 150µV. Process corner simulations performed to investigate the reference voltage dependence on the variation in the process. The Simulated Result of output voltage vs. temperature with process corner are depicted in figure.3(c). Generally, IoT applications are battery operated systems, and supply voltages are less noisy. To analyse power supply noise effect on the voltage reference circuit to power supply noise the PSR simulation performed. Figure.3(d) shows a different value of PSRR at different frequencies and achieved PSR of -33db@100 HZ.

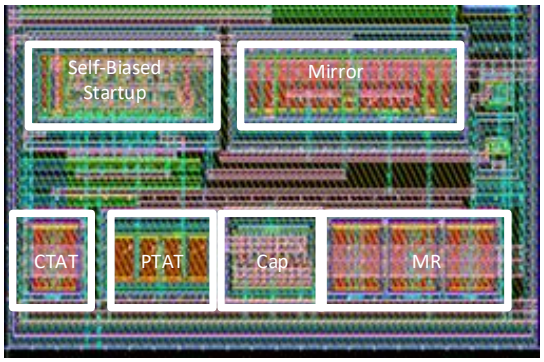


Fig. 4 Layout diagram of proposed work

Conclusion: A CMOS voltage reference below threshold (CVR) It has been demonstrated to use a low power consumption in the 0.18 µm SCL CMOS process. The suggested circuit operates with low voltage and little power by utilising MOS transistors with subthreshold working regions. Using subthreshold region functioning, a temperature-independent voltage reference circuit for nano-power devices is created. The suggested circuit generates 770 mV at room temperature and achieves temperature sensitivity of 100 ppm/°Cover a temperature range of -40 °C to 125 °C utilising a set of 0.18 m SCL's standard CMOS process settings and 1.8 v voltage supply. The device uses less than 50 nW of electricity and takes up a chip size of 30 µm by 30 µm.

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