

Dynamic on-state resistance instability characterization of a Multi-chip-GaN MIS-HEMTs Cascode power module

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January 4, 2023

Abstract

The dynamic on-state resistance instability of a high-current cascode multi-GaN-chip power module under high frequency and voltage switching conditions is demonstrated in this paper. The presented double pulse test (DPT) topology is utilized to evaluate switching dependencies on voltage, current, and frequency, showing its versatility in investigating the switching instability of the device. The extended defects in the buffer layer resulted in a decrease in dynamic on-state resistance (RDS-ON) under hard switching conditions. Despite this, no noticeable RDS-ON degradation occurs under harsh switching conditions due to electron de-trapping. This study comprehensively analyzes the dynamic stability of a multi-GaN-chip cascode module with devices.

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Abstract. The dynamic on-state resistance instability of a high-current cascode multi-GaN-chip power module under high frequency and voltage switching conditions is demonstrated in this paper. The presented double pulse test (DPT) topology is utilized to evaluate switching dependencies on voltage, current, and frequency, showing its versatility in investigating the switching instability of the device. The extended defects in the buffer layer resulted in a decrease in dynamic on-state resistance (R_{DS-ON}) under hard switching conditions. Despite this, no noticeable R_{DS-ON} degradation occurs under harsh switching conditions due to electron de-trapping. This study comprehensively analyzes the dynamic stability of a multi-GaN-chip cascode module with devices.

Introduction: Gallium Nitride (GaN)-based high-electron-mobility transistors (HEMTs) have been superior candidates in power electronics applications for many years due to their low on-resistance, fast switching speed, high-temperature, high power, and high frequency operating characteristics [1,]. Currently available single-chip E-mode GaN power devices usually have a restricted gate voltage swing, requiring precision control in power conversion applications to avoid spikes [2]. Therefore, paralleling GaN HEMTs in cascode configuration has become a practical choice to achieve high power capability with large gate swing for GaN-based power devices [3, 4].

In earlier studies, a comprehensive analysis of the multi-GaN-chip cascode power module fabrication method, thermal performance, and the potential use of GaN power switches was presented [5]. As part of the device-level stability analysis, trapping-related instabilities were examined under a specific constant bias, e.g., constant gate bias, constant drain bias, etc. In our earlier studies [6], pulsed, and prolonged gate bias or bias temperature instability are reported. In this paper, a 400 V power module which consists of two switching elements that connect multi-GaN-chips (four GaN chips) with low voltage Si MOSFETs in series is implemented for system-

level stability under hard switching conditions, which is shown in Fig 1.



Fig 1 Epoxy cased multi-GaN cascode power module device (8-GaN chips & 2-Si chips) with gate, source, and drain contacts.

For decades, GaN-based power devices have been developed and commercialized, showing their potential for use in consumer electronics [1]. However, various GaN devices suffer from dynamic on-state resistance (R_{DS-ON}) degradation during system-level operations, which hinders their practical use [7]. Electron trapping or detrapping from surface traps and/or buffer traps caused by the high electric field across the device under hard switching conditions is one of the reasons. Furthermore, hot electron generations in the channel are injected at the surface or in the buffer stack, which could be another cause of R_{DS-ON} degradations. Despite numerous advanced technologies that mitigate the current collapse, dynamic R_{DS-ON} degradation remains a major concern for commercial GaN devices.

In this work, the dynamic R_{DS-ON} degradation of the novel multi-GaN-chip cascode power module is investigated to predict its accurate performance. To assess the switching dependencies of the device under test (DUT) such as voltage, current, frequency, and duty cycle, the double pulse test (DPT) method was employed.

Topology and Methodology: The DPT is a typical method for assessing the dynamic R_{DS-ON} of power devices for switching under hard conditions [8]. At the second pulse with the required voltage and current, the switching transient response of the DUT can be recorded. Furthermore, the DPT method achieves various switching dependencies for dynamic R_{DS-ON} degradation studies. Fig. 2a shows the DPT schematic circuit for the hard switching conditions used in this study.

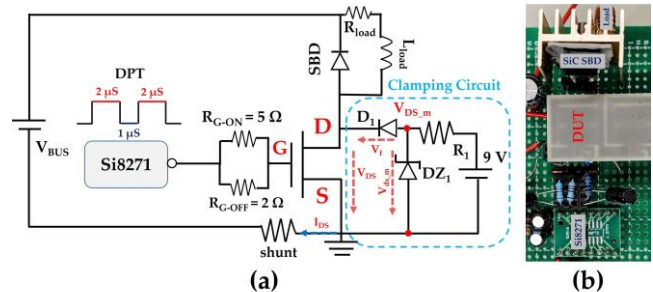


Fig 2 (a) Schematic circuits of the double-pulse tester with a clamping circuit and (b) test board.

A bulk capacitor (C_{bulk}) with a huge capacitance of 520 μF was selected for fast transmission of electric energy and to ensure the input power voltage was steady. The Schottky barrier diode (SBD) provides freewheeling communication

for the inductive load in this system. Inductive and resistive loads (RL) were integrated to provide a low resistance and inductance current path to the DUT. An isolated half-bridge driver IC Si8271 was chosen from the test board to offer quick propagation time and a broad supply range [9]. The switching speed is controlled by external resistors such as R_{G-OFF} of 2 Ω and R_{G-ON} of 5 Ω .

A clamping circuit was added to prevent high off-state voltage while accurately determining the low on-state drain voltage, which relies on a Zener diode (D_{Z1}) and a SiC Schottky diode (D_1) with high voltage and fast switching and zero recovery [9]. A high voltage is applied between the source and drain, the D_1 in the clamping circuit gets reverse biased, and current flows through a D_{Z1} , resistance (R_1), and a low-power supply (9 V). The clamping voltage is used as the measured voltage because it is substantially smaller than the off-state voltage of the real DUT. The on-state drain voltage was derived by subtracting the measured drain-to-source value (V_{DS-m}) from the diode D_1 turn-on voltage (V_{F-D1}).

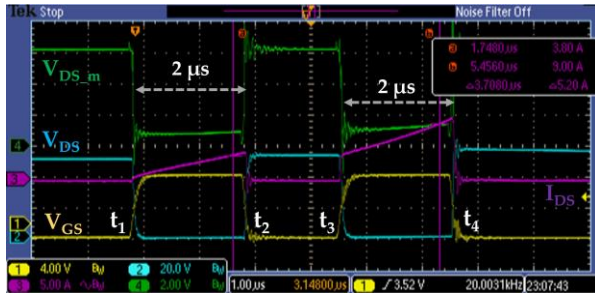


Fig 3 The real waveform of tested gate voltage (V_{GS}), off-state drain voltage (V_{DS}), drain current (I_{DS}) and measure clamping voltage (V_{DS-m}).

Fig. 3 displays the switching waveform of the DUT at 50 V off-state voltage, and the yellow, light blue, purple, and green lines indicate the gate voltage (V_{GS}), the drain voltage (V_{DS}), the drain current (I_{DS}), and the clamping voltage (V_{DS-m}). At t_1 , the DUT switches to on-state and is maintained for 2 μs until t_2 . The load current (I_L) through the DUT keeps rising as the inductive load charges up. At t_2 , the current through the DUT increased to 4 A. Afterwards, a SiC SBD is used as a freewheeling diode, while the DUT is switched off for 1 μs . Later, the DUT turns on again for another 2 μs under the second pulse and the current increases to 9 A at the end of the second pulse at t_4 . With a measuring delay time of 300 ns, we observed dynamic R_{DS-ON} of the DUT under the second pulse. With various switching voltages, the load current at the end of the initial on-state pulse can be maintained at the same value by adjusting the load inductance.

Results: To our knowledge, this is the first study demonstrating effective double pulse switching up to 300V using multi-GaN-chip cascode devices at 300kHz and 60% duty cycle. Fig. 4a shows the observed dynamic R_{DS-ON} of the DUT at different off-state voltages from 50 to 300 V with a 50 V step value. By adjusting the external RL-load, the I_{DS} is kept constant at 4 A for each switching

voltage. Additionally, a 20 min test interval is utilized to fully release the trapped electrons to evaluate the accuracy of the dynamic R_{DS-ON} for each off-state voltage. A very minimal decrease in R_{DS-ON} devices were observed with increasing off-state voltage.

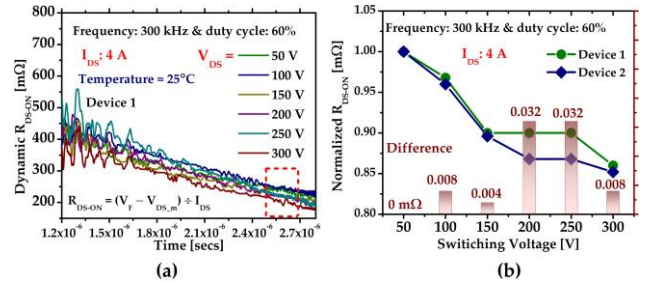


Fig 4 (a) Dynamic R_{DS-ON} of device1 with different off-state voltage from 50 to 300 V and $I_{DS} = 4$ A. (b) Normalized R_{DS-ON} and difference between both devices from module.

Fig. 4b shows the normalized dynamic R_{DS-ON} for both devices from the cascode power module over various switching voltages and the differences between them. Normalized R_{DS-ON} decreases from 1 m Ω to 0.85 m Ω as the switching voltage increases. The device has a high R_{DS-ON} despite its low off-voltage (50 V), which correlates with GaN HEMTs in general [8]. As the off-state voltage increases from 100 to 300 V, the dynamic R_{DS-ON} degradation reduces and becomes more stable with the lowest value of 215 m Ω . In addition, the difference between the two devices is negligible (0.032 m Ω), so the cascode power module has the same characteristics regardless of the off-state voltage.

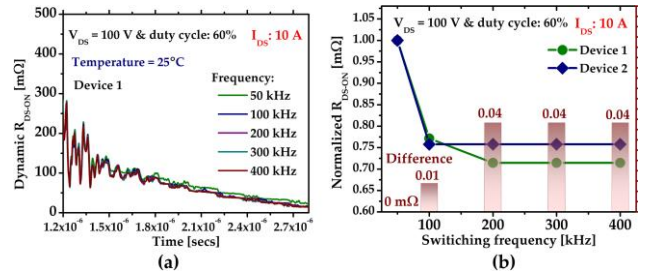


Fig 5 (a) Dynamic R_{DS-ON} of device1 for different switching frequency from 50 to 400 kHz with $V_{DS} = 100$ V and $I_{DS} = 10$ A. (b) Normalized R_{DS-ON} and difference between both devices.

Fig. 5a shows the dynamic R_{DS-ON} for different switching frequencies of the DUT with $V_{DS} = 100$ V and $I_{DS} = 10$ A. At low switching frequencies, the device exhibits slightly high R_{DS-ON} , but as the switching frequency increases, R_{DS-ON} decreases and becomes stable. Fig. 5b confirms the same characteristics of both devices from the cascode module regardless of various switching frequencies. Furthermore, neither device showed discernible R_{DS-ON} degradation for high frequency switching (400 kHz). Fig. 6a shows the dynamic R_{DS-ON} of the DUT for different I_{DS} from 2 to 10 A with $V_{DS} = 100$ V and 300 kHz. In response to an increase in switching current, the R_{DS-ON} decreases as well. Fig. 6b shows the normalized dynamic R_{DS-ON} for increasing I_{DS} at different off-state voltages. When the I_{DS} value was more than 4 A, the DUT observed a reduction of R_{DS-ON} from 1 m Ω (50 V) to 0.6 for 300 V; 6 A, 0.31 m Ω for 300 V; 8 A,

and 0.01 mΩ for 300 V; 10 A. The R_{DS-ON} of the DUT decreased and became unstable with increasing off-state voltage and current switching conditions. Additionally, Fig. 6b verifies that both devices from the cascode module have the same characteristics, regardless of the various off-state voltages and currents.

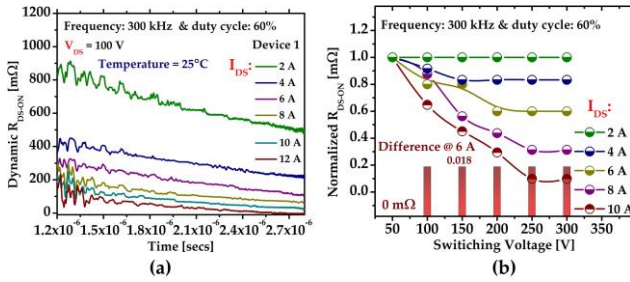


Fig 6 (a) Dynamic R_{DS-ON} of device1 for different switching current from 2 to 12 A with $V_{DS} = 100$ V and 300 kHz. (b) Normalized R_{DS-ON} and difference between both devices.

Discussions: Recently, researchers have studied buffer, barrier, and surface trapping mechanisms that generate traps during device growth phases [10]. A highly resistive buffer layer is created by doping carbon, resulting in extended defects from carbon compensations [11]. Fig. 7a show the buffer-related traps in GaN HEMT. Trap states that are present in the bulk, near the 2DEG, or at the surface often promote the trapping/detrapping processes that lead to R_{DS-ON} degradation.

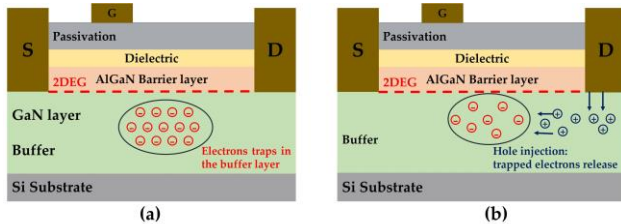


Fig 7 (a) Schematic of the buffer-related traps in the GaN HEMT and (b) Hole injection from drain due to high channel current.

Under hard switching conditions, the dynamic R_{DS-ON} decreases differently from previous reports. During high current switching, trapped electrons can be reduced. Fig. 7b shows the hole injection from drain due to high channel current. At harsh switching conditions, the observed decrease in dynamic on-resistance can be explained by the "hole injection" approach to charge storage [12]. As a result of a highly carbon-doped buffer layer and leakage path between the source and drain, the hole current can flow from the drain into the buffer layer. Vertical leakage holes from the drain into the buffer layer release trapped electrons under high channel current, resulting in the decrease of dynamic R_{DS-ON} . As channel current increases, the number of emitted electrons rises, which leads to unstable R_{DS-ON} .

Conclusion: In this paper, we investigated the dynamic on-resistance behavior of a multi-GaN-chip cascode power module under hard-switching conditions. With field plate technology in GaN HEMT, the electron trapping effect was minimized. The performance of dynamic R_{DS-ON} appears non-monotonic, indicating constant drops as off-state

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voltage, switching frequency, and current increase. All the results suggest that R_{DS-ON} is dropped as a result of vertical leakage holes from the drain into the buffer layer releasing trapped electrons under high channel current. A multi-GaN-chip cascode power module requires more quantitative research to fully understand its dynamic characteristics.

Received: xx January 2021 Accepted: xx March 2021
doi: 10.1049/ell2.10001

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