A Single-event Transient Mitigation Technique for Bandgap Reference Utilizing in Space Application

Qiangguo Zhao[1], Jingtian Liu[2], BIn Liang[1], Jianjun Chen[1], Yaqing Chi[1], Deng Luo[1], Yang Guo[1], and Hanhan Sun[1]

[1]National University of Defense Technology College of Computers
[2]National University of Defense Technology

January 3, 2023

Abstract

This paper proposes a radiation-hardened-by-design (RHBD) technique targeting single-event transient (SET) mitigation in bandgap reference (BGR) circuits. The dual modular redundancy (DMR) technique used for BGR ensures correct output voltage to the subsequent circuits. The BGR output voltage is detected and clamped by two threshold voltages and time-delayed switches further isolate SET pulses. The proposed BGR circuit was fabricated in 28 nm bulk CMOS process. Laser experiments illustrate that SET perturbation is almost eliminated when laser energy is up to 1 nJ. The RHBD BGR is proven to be good substitute for space applications.

A Single-event Transient Mitigation Technique for Bandgap Reference Utilizing in Space Application

Qiangguo Zhao, Jingtian Liu, Bin Liang, Jianjun Chen, Yaqing Chi, Deng Luo, Yang Guo, and Hanhan Sun*

This paper proposes a radiation-hardened-by-design (RHBD) technique targeting single-event transient (SET) mitigation in bandgap reference (BGR) circuits. The dual modular redundancy (DMR) technique used for BGR ensures correct output voltage to the subsequent circuits. The BGR output voltage is detected and clamped by two threshold voltages and time-delayed switches further isolate SET pulses. The proposed BGR circuit was fabricated in 28 nm bulk CMOS process. Laser experiments illustrate that SET perturbation is almost eliminated when laser energy is up to 1 nJ. The RHBD BGR is proven to be good substitute for space applications.

Introduction: Bandgap reference (BGR) is a critical building block widely adopted in integrated circuits (ICs) [1], which provides robust and precise voltage reference over process, supply voltage, and temperature (PVT) variations to subsequent modules, such as low-dropout regulators. The robustness requirement is more challenging in space environment due to exposure to the wide spectrum of energetic photons and particles [2]. If heavy ions inject into the BGR circuit and produces a transient at its output voltage, all subcomponents relying on such reference are disrupted, resulting in signal corruption and even system failure. Since the radiation performance of bandgap circuit is essential to whole system, it is imperative to enhance BGR radiation tolerance.

The related research on the single-event transient (SET) effects of the bandgap reference circuit were reported in [3-7]. The circuit-level radiation-hardened-by-design (RHBD) techniques, such as the guard ring technique [3], the triode reverse connection [4], and the inverse-mode transistors [5], were adopted in SiGe BiCMOS technology. The suppression of SET pulses was also realized by pulse quenching [6] and DC signal isolation [7] in bulk CMOS process. However, there are currently few papers on the module-level RHBD techniques for mitigating SET effects.

This paper presents a module-level technique for BGR stabilization. The dual modular redundancy (DMR) technique is used to ensure the correct output voltage to the subsequent circuits. Laser experiment was conducted on the proposed BGR circuit fabricated in 28 nm bulk CMOS process, illustrating that the SET perturbation is almost eliminated. This provides a new guidance for SET mitigation on constant DC level and is widely applicable for bandgap radiation-hardening design.

Circuit design: The structure of the proposed BGR is shown in Figure 1. If a disturbance is induced with a heavy-ion striking at the sensitive nodes of the bandgap block and its output exceeds the high (V_{high_thresh}) and low (V_{low_thresh}) threshold voltage, this anomaly can be captured and triggers the bandgap temporarily disconnecting to the output. Therefore, SET-induced perturbations cannot propagate to the subsequent modules. However, the output is floating with bandgap disconnecting to output. Crosstalk and noise from the substrate and other modules can easily destroy the voltage at the output node.

The issue above can be solved by adding an identical bandgap block. Two bandgaps provide the same DC level simultaneously during normal operation. If one of the bandgaps is subjected by the energetic particle and its output goes beyond the normal region, the switch connecting the bandgap and the output would be triggered "off", which isolates the abnormal signal from the core circuit. Meanwhile, one unaffected bandgap provides correct voltage reference to other functional blocks. The redundancy technique is adopted since heavy ion hits only one node at one time. Theoretically, this redundancy design can totally suppress SET on the BGR output.

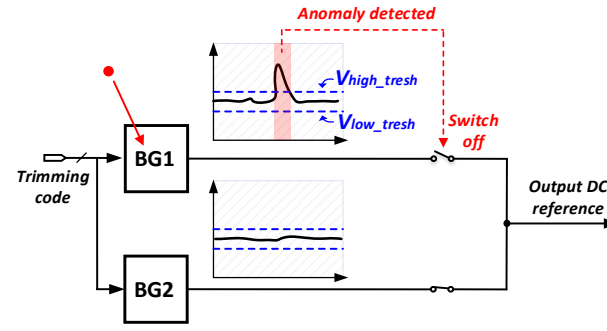

Fig. 1 *The outputs of BGR clamped by threshold voltages and filtered out if anomaly detected.*

Figure 2(a) presents a typical BGR circuit. The core circuit features a zero temperature coefficient (TC) output voltage, typically realized by adding two currents with opposite TCs and proper weighting [8]. The bipolar transistors' base-emitter voltage exhibits a negative TC and the difference between two bipolar transistors' base-emitter voltages with unequal current densities has a positive TC.

Due to the "virtual short", the amplifier forces nodes V_n and V_p to be approximately equal. Thus, the current flowing through the resistance R_2 is given by:

$$I_2 = \frac{V_{BE1}}{R_2}, \quad (1)$$

which is inversely proportional to absolute temperature (IPTAT). The bipolar transistor Q1 is only one, while Q2 consists of N paralleled bipolar transistors, so the current flowing through the resistance R_1 is given by:

$$I_1 = \frac{V_{BE1}-V_{BE2}}{R_1} = V_T \ln\frac{N}{R_1}, \quad (2)$$

which is proportional to absolute temperature (PTAT). The thermal voltage can be given by:

$$V_T = \frac{kT}{q}, \quad (3)$$

where k is Boltzmann constant, T is thermodynamic temperature, and q is the charge constant value. The PMOS transistors M1~M3 have the same size, and the drain current of M2 is given by:

$$I_0 = I_1 + I_2 = \frac{V_{BE1}}{R_2} + \frac{V_T \ln N}{R_1} = \frac{V_{BE1}+V_T \ln N \cdot \frac{R_2}{R_1}}{R_2}. \quad (4)$$

So, the output voltage V_{init} of the BGR circuit can be calculated by multiplying the drain current of transistor M3 by the load resistance R_3:

$$V_{init} = \left(V_{BE1} + V_T \ln N \cdot \frac{R_2}{R_1}\right) \cdot \frac{R_3}{R_2}. \quad (5)$$

As for the output zero temperature coefficient of the BGR circuit:

$$\frac{\partial V_{bg}}{\partial T} = \frac{\partial V_{BE1}}{\partial T} + \frac{R_2}{R_1} \cdot \frac{k}{q} \ln N \equiv 0. \quad (6)$$

V_{init} can be designed to be a constant voltage reference and independent of temperature by choosing appropriate ratio N, and resistances R_1 and R_2. The load resistance R_3 can be dynamically configured through an external digital code, so that the output voltages meet the requirements of different reference voltage values.

Figure 2(b) illustrates the RHBD bandgap system using DMR technique. Two identical bandgap blocks are included in two uniform branches and simultaneously provide identical DC reference to the output during normal operation. In each branch, the signal V_{init} produced by bandgap core block (BG) is buffered out

with a unity-gain amplifier (Amp), which boosts the driving ability. Then each V_{amp} passes through two transmission gates (TG and TG') to filter abnormal DC level and finally merge to provide the output voltage V_{out}. The trigger signals (S and S') for transmission gates are determined by a 4-bit threshold trimming code and the amplifier output.

As for the digital configuration, the least significant-bit (LSB) of threshold voltage regulation is 0.9V/ (2^4+1) = 52.9 mV, which clamps the bandgap output voltage within this range. During normal operation, S and S' are remaining "1" and transmission gates are turned on. If one of the bandgap core blocks is striken by heavy ion and its output temporarily goes beyond the threshold voltages, the comparators (Comps) would detect this anomaly and trigger S and S' signals to change from "1" to "0". As a result, transmission gates are turned off and prevent the SET signal from propagating to the output (V_{out}). Time delay between S and S' signals is controlled by the semi-custom delay block (Delay), and further contributes to SET pulse isolation. The S signal returns to "1" after bandgap voltage recovering to be within the threshold range, but S' finally returns to "1" until 500 ns after S signal jumping to high level. This provides more time for bandgap recovery and benefits the reduction of output voltage deviation.

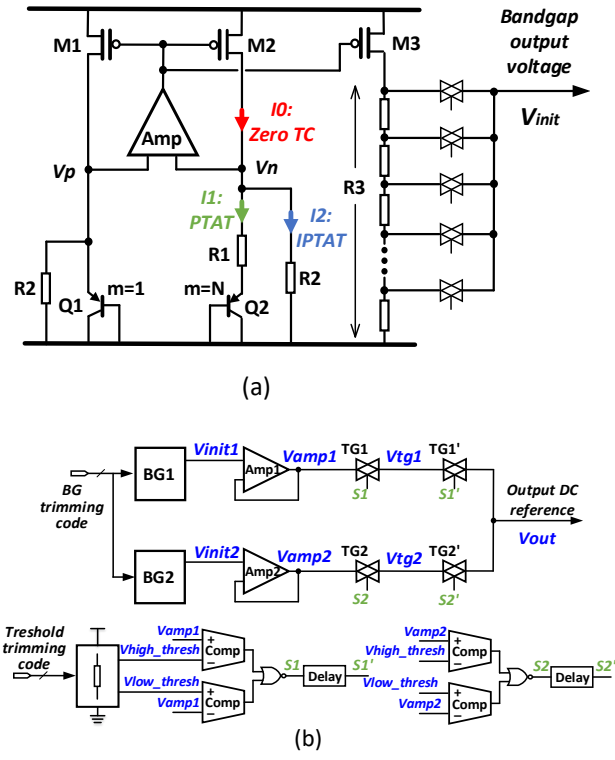

Fig. 2 *Schematic of BGR circuit. (a) A typical bandgap core block implemented with bipolar transistors. (b) The schematic of the RHBD bandgap circuit using DMR technique.*

Spice-level simulations: As a simple approximation, the disturbance caused by heavy-ion striking is modeled by double-exponential current source, which can represent the transient effect generated by the incident particles [9,10]. Then the corresponding response of the circuit is provided for SET analysis. The deposited charge by the current source is 200fC. The time constants, the rising time and falling time, are calibrated as 20 ps and 200 ps respectively.

In the simulation, a SET hits at the output of bandgap core block in the first branch to emulate the radiation effect in harsh environment. During normal operation, bandgap provides a precise 542 mV reference voltage to the output regardless of PVT variations. Therefore, the threshold trimming code is set to 9 and 10, with corresponding 529 mV and 582 mV high and low threshold voltages, respectively. As shown in Figure 3, V_{init1} suffers from a large positive-going disturbance with current source injecting at M3 drain node in the first branch. This perturbation is copied to V_{amp1}, which largely exceeds the high threshold limit. This triggers the comparator which compares the V_{amp1} with V_{high_thresh} to output "1" and signals S1 and S1' after NOR gates jumping to "0", which turns off the TG1 and TG1'. Therefore, V_{tg1} suffers from a slight voltage fluctuation, mainly resulting from the switching of transmission gate. After bandgap voltage returns to the threshold voltage range, S1 again jumps to "1" and TG1 restores to be conduction state. V_{tg1} signal follows the V_{amp1} tail and is likely to cause output voltage deviation.

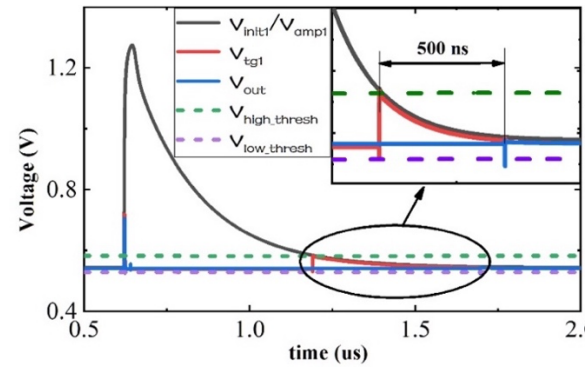

Fig. 3 *Spice simulation results of the anti-SET property of the proposed technique.*

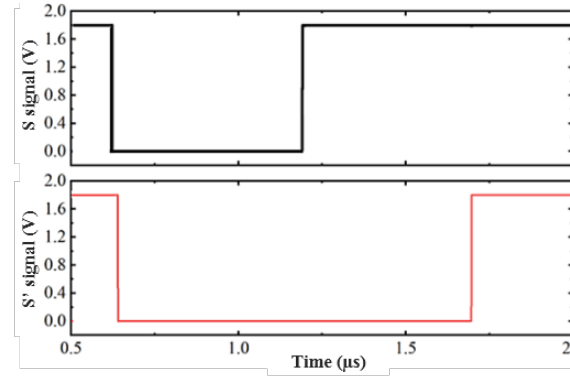

Fig. 4 *Waveforms of S1 and S1' signals in the spice simulation when the particle strikes.*

The maximum value of this deviation is one LSB of the threshold voltage. By adding another transmission gate after TG1', the control signal of the transmission gate detects the logic low of S1 and extends the low level by 500 ns, which can prolong the recovery time for the whole system, thereby further solving the SET tailing problem, as shown in the Figure 4. When the BGR circuit is hit by a single event, the SET perturbation is completely unable to be transmitted to the output due to the proposed radiation hardened circuits, and no voltage perturbation can be detected on V_{out}.

Experimental results: To test the validity of the proposed technique, a RHBD bandgap circuit and a normal bandgap circuit are designed and fabricated in 28 nm bulk CMOS process with 1.8 V power supply voltage for IOs and 0.9 V for core circuits. The test

chip was packaged by flip-chip technique, so the substrate has been ground to about 50 μm before irradiation, and the backside of the chip was incident by the particles. The printed circuit board (PCB), with the test chip being welded, was used for the test execution.

An oscilloscope located outside is employed to detect the SET on the output of the bandgap circuit, which can "hold" instantaneous waveforms when detecting abnormal signals. To exclude the inherent jitter from ambient and internal noise, the trigger thresholds of waveform measurement and storage is carefully set with the voltage deviation up to 1.5% of the reference voltage. The data are analyzed and processed offline.

Pulsed laser is a powerful tool for characterizing the radiation response of the test chips [11,12]. Pulsed laser experiments possess micron-level focusing resolution and allow injecting SET charges in a specific region. During the experiment, four boundary corners of the BGR were located, and the core region of the RHBD BGR was scanned to study its radiation response and identify the sensitive area. The laser energy used in the experiments can be equivalent to the linear energy transfer (LET) value in the heavy-ion experiments, allowing quantitative analysis of the SET susceptibility of the specific regions.

The pulsed laser experiment was conducted at National Space Science Center, Chinese Academy of Sciences, Beijing, China [11,12]. To prevent the metal layer on the front side of the test chip from obstructing the laser, the pulsed laser was illuminated at 1064 nm laser wavelength from the backside of the chip, and high-power pulses of sub-bandgap light wavelength were used to generate charges in the target area through two-photon absorption (TPA) [13]. The chip substrate was partially thinned down to achieve efficient laser-induced charge generation rates. The laser spot size used was about 1.5×1.5 μm^2.

For SET susceptibility characterization, the initial laser energy and the increment laser energy are set to 200 pJ during the experiment. SETs in the unhardened BGR were always captured by the oscilloscope with the similar shapes and increasing amplitudes. While the radiation-hardened BGR survived up to 1 nJ laser irradiation. Table 1 summarizes the worst laser test results in both the hardened and unhardened BGR circuits for comparison. The hardened BGR improved the SET tolerance capability to 1 nJ at least. This indicates that the SET is significantly mitigated by the proposed RHBD techniques in comparison to its original counterpart.

Table 1: *Worst cases of the laser-induced perturbation.*

Laser energy (pJ)	SET amplitude in un-hardened circuit (mV)	SET amplitude in hardened circuit (mV)
200	202	-
400	563	-
600	751	-
800	896	-
1000	954	8

Conclusion: In this paper, a module-level RHBD technique is proposed for SET mitigation in BGR circuit. The adopted DMR technique ensures the correct reference voltage when one BGR block is hit by the high-energy particle in the space radiation environment at a time. Laser experiments demonstrate that the proposed RHBD technique significantly reduces the SET duration up to 1 nJ laser energy.

Acknowledgments: This work is supported by the National Natural Science Foundation of China (Grant No. 61974163, and No. 62174180).

Qiangguo Zhao, Jingtian Liu, Bin Liang, Jianjun Chen, Yaqing Chi, Deng Luo, Yang Guo, and Hanhan Sun (*College of Computer, National University of Defense Technology, Changsha 410073, China*)

E-mail: hhsun108@163.com

Qiangguo Zhao: also with *College of microelectronics, Xi'an Jiaotong University, Xi'an 710049, China*.

Jingtian Liu: also with *National Innovation Institute of Defense Technology, Academy of Military Sciences PLA China, Beijing 100071, China*.

References

1. Kuijk K. E.: 'A precision reference voltage source', *IEEE Journal of Solid-State Circuits*, 1973, **8**, (3), pp. 222-226, doi: 10.1109/JSSC.1973.1050378
2. Ferlet-Cavrois V., et al: 'Single Event Transients in Digital CMOS—A Review', *IEEE Transactions on Nuclear Science*, 2013, **60**, (3), pp. 1767-1790, doi: 10.1109/TNS.2013.2255624
3. Najafizadeh L., et al: 'Single Event Transient Response of SiGe Voltage References and Its Impact on the Performance of Analog and Mixed-Signal Circuits', *IEEE Transactions on Nuclear Science*, 2009, **56**, (6), pp. 3469-3476, doi: 10.1109/TNS.2009.2034159
4. Andreou C. M., et al: 'Low-Power, Subthreshold Reference Circuits for the Space Environment: Evaluated with γ-rays, X-rays, Protons and Heavy Ions', *Electronics*, 2019, **8**, (5), pp. 562, doi: 10.3390/electronics8050562
5. Cardoso A.S., et al: 'Single-Event Transient and Total Dose Response of Precision Voltage Reference Circuits Designed in a 90-nm SiGe BiCMOS Technology', *IEEE Transactions on Nuclear Science*, 2014, **61**, (6), pp. 3210-3217, doi: 10.1109/TNS.2014.2358078
6. Andreou C.M., et al: 'Single Event Transients and Pulse Quenching Effects in Bandgap Reference Topologies for Space Applications', *IEEE Transactions on Nuclear Science*, 2016, **63**, (6), pp. 2950-2961, doi: 10.1109/TNS.2016.2611639
7. Ren Y., et al: 'An RHBD Bandgap Reference Utilizing Single Event Transient Isolation Technique', *IEEE Transactions on Nuclear Science*, 2016, **63**, (3), 1927-1933, doi: 10.1109/TNS.2016.2554104
8. Razavi B,: 'Design of analog CMOS integrated circuits' (McGraw-Hill, New York, USA, 2001, second edition)
9. Warren K. M., et al: 'Integrating Circuit Level Simulation and Monte-Carlo Radiation Transport Code for Single Event Upset Analysis in SEU Hardened Circuitry', *IEEE Transactions on Nuclear Science*, 2008, **55**, (6), pp. 2886-2894, doi: 10.1109/TNS.2008.2006481
10. Black D. A., et al: 'Modeling of Single Event Transients with Dual Double-Exponential Current Sources: Implications for Logic Cell Characterization', *IEEE Transactions on Nuclear Science*, 2015, **62**, (4), pp. 1540-1549, doi: 10.1109/TNS.2015.2449073
11. Yuan H., et al: '28nm Fault-Tolerant Hardening-by-Design Frequency Divider for Reducing Soft Errors in Clock and Data Recovery', *IEEE Access*, 2019, **7**, pp. 47955-47961, doi: 10.1109/ACCESS.2019.2906884
12. Yuan H., et al: 'An SEU/SET-Tolerant Phase Frequency Detector with Double-Loop Self-Sampling Technology for Clock Data Recovery', *IEEE Transactions on Nuclear Science*, 2019, **66**, (7), pp. 1483-1490, doi: 10.1109/TNS.2019.2922673
13. McMorrow D., et al: 'Three-dimensional mapping of single-event effects using two photon absorption', *IEEE Transactions on Nuclear Science*, 2003, **50**, (6), pp. 2199-2207, doi: 10.1109/TNS.2003.820742