A wide input range, external capacitor-less LDO with fast transient response

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Abstract

A high-voltage, external capacitor-less low-dropout regulator (HVLDO) with a transient enhancement loop is presented in this work. The proposed HVLDO is designed with high withstand voltage LDMOS transistors and a transient enhancement loop is proposed to properly inject or sink current to/from the gate and output nodes of the power transistors to achieve fast transient response under wide load range conditions and high stability. This HVLDO is fabricated in 0.5 μm SOI BCD process with an active area of 0.29 mm2. It operates over an input voltage range of 5.2 to 20 V, provides an output voltage of 5 V and a maximum load of 100 mA, while supporting load capacitances from 0 pF to 1 μF. Measurements show that this design has a line regulation of 0.88 mV/V and a load regulation of 0.22 mV/mA. The proposed HVLDO features fast line transient response of 60/20 mV@9.8 V/μs, fast load transient response of 30/70 mV@100 mA/μs, and recovery time of 2 μs without external capacitors. Compared with the prior art, this work achieves the best transient FOM of 12.19 fs.

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Introduction: In recent years, battery-powered equipment and portable electronic products such as automotive and telecom electronics have developed rapidly, hence the demand for high voltage power management

systems is also increasing. Compared with switching power supply regulators and charge pump power supply regulators, low dropout linear regulators have the advantages of small area, small ripple, high power supply noise rejection ratio and fewer external components, which make them widely used in high-precision electronic products [1].

However, traditional LDOs have a narrow input supply range (typically 2-5 V) and require external output capacitors in the μF range for improved transient response and good stability. But this requires extra external pins and cannot be integrated into the whole chip. To remove external components and reduce system size, capacitorless LDOs are proposed in [2-7]. But all previous LDOs have trade-offs between wide input and load current ranges, the need for large off-chip capacitors, and output transient response. In this letter, a capacitorless HVLDO with transient enhancement loop is proposed. Benefiting from the transient enhancement loop, the proposed LDO has optimized line and load regulation performance and fast load transient and line transient response.

LDO design: Fig. 1 shows the topology of the proposed HVLDO. The pre-regulator circuit is designed to power the bandgap reference circuit to improve PSR. The bandgap reference provides proper biasing for the LDO and achieves a temperature coefficient of 13.15 ppm/°C, over a wide temperature range of -40-150°C. Transient-enhanced linear regulator is the core part, which can output regulated voltages during load and supply voltage transients.

Fig. 1 *Topology of the proposed HVLDO.*

The circuit implementation of the proposed transient enhancement linear regulator is presented in Fig. 2, including the bias generation circuit, error amplifier, transient enhancement loop, and power output stage. Bias generation circuit generates proper bias voltage and current for LDO. The error amplifier detects the change of the output voltage through the feedback resistors R1 and R2, compares Vfb with the reference voltage Vref, then controls the gate voltage of the power transistor M0 to stabilize the output voltage. In particular, the design proposes a transient enhancement loop, which provides an additional fast control loop for the gate of M0 while acting as an active capacitor to provide transient inject or sink current to/from the output point, enhancing transient response without off-chip capacitors.

Fig. 2 *Schematic of the proposed HVLDO with transient enhancement loop.*

Error Amplifier: The error amplifier is a symmetrical transconductance amplifier (OTA) consisting of M1-M11. M10 and M11 provide higher DC bias for the source stage of M8, so that the output of the OTA can drive the P-type power output transistor M0 with a suitable common-mode voltage. The power output stage consists of power transistor M0, feedback resistor network R1, R2 and 5 pF Miller compensation capacitor Cc and zeroing resistor Rc. The output power transistor M0 has an aspect ratio of 10 mm/360 nm to provide 100 mA at a voltage drop of 200 mV. C_L and R_L are the load capacitance and load resistance. The error amplifier detects the change of the output voltage and compares Vfb with the reference voltage Vref, then controls the gate voltage of the M0 to stabilize the output voltage.

Transient Enhancement Loop: The circuit implementation of the proposed transient enhancement loop is shown in Fig. 2, consisting of 18 transistors M12-M25, M_{PU}, M_{PD}, M_{GPU}, M_{GPD}, including the M0 gate transient enhancement control loop and output grade active capacitors. Specifically, the two pairs of operational amplifiers M12-M16 and M19-M23 detect the output Vout change through the feedback point Vfb. The OTA control transistor M_{GPU} (or M_{GPD}) injects (or pulls out) a transient current I_{GPU} (or I_{GPD}) to the gate of M0, thereby pulling the gate voltage of M0 high (or low). The gate transient enhancement control loop of M0 can shorten the transient response time, replace the traditional analog buffer to minimize the quiescent current. The active capacitor shares the OTA with the gate transient control loop. Inverter M17-18 (or M24-25) controls M_{PD} (or M_{PU}) to pull out (or inject) the transient current I_{PD} (or I_{PU}) out of the LDO output for instantly suppressing ΔVout, which achieves the transient response enhancement.

The GBW of the transient enhancement circuit is designed to be higher than that of the error amplifier to meet the corresponding needs of fast transients. Set the width to length ratio of M17-18 and M24-25 in

Fig. 2 to adjust their inversion thresholds (corresponding to INV1 and INV2 in Fig. 1) so that M_{PU} and M_{PD} are turned off in steady state and only work for transient response , which can improve stability and reduce power consumption. Set the size of M_{PU} and M_{PD} to 60:1 of M0 to avoid excessive transient current compensation. In order to verify the stability of the HVLDO, the stability of the HVLDO under different load conditions is simulated, and the results are shown in Fig. 3. It can be seen that PM is 74.2 deg@0 mA, 74.5 deg@1 mA and 68.4 deg@100 mA. The circuit has good stability under all load conditions.

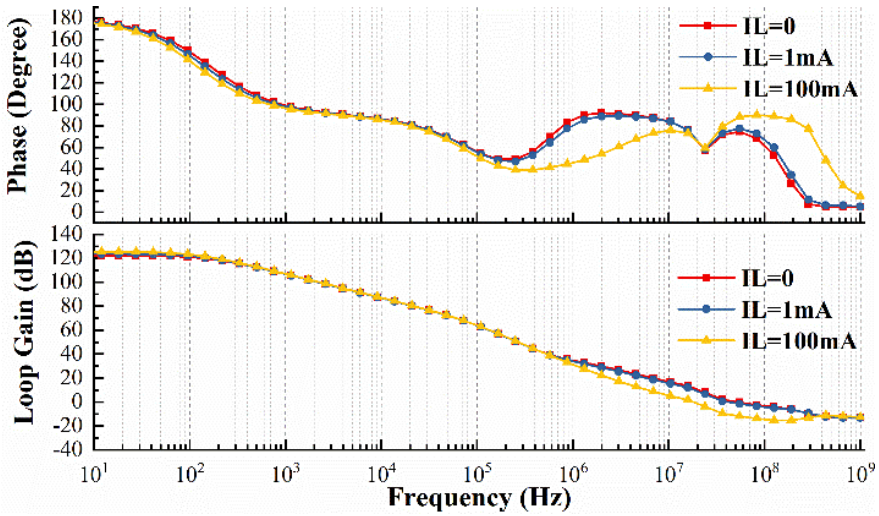

Fig. 3 Stability simulation results under different load conditions.

Measurement results: The proposed HVLDO was implemented in 0.5 μm SOI BCD process with an active area of 835μm*347μm (without pads) as shown in the chip micrograph in Fig. 4. This HVLDO delivers a maximum load of 100 mA. The ground current of this HVLDO is 243.8 μA when the load current increases from 0 to 100 mA. The peak current efficiency achieves 99.75%.

Fig. 5 shows the measurement results of line regulation

Fig. 4 *Chip micrograph of the proposed HVLDO.*

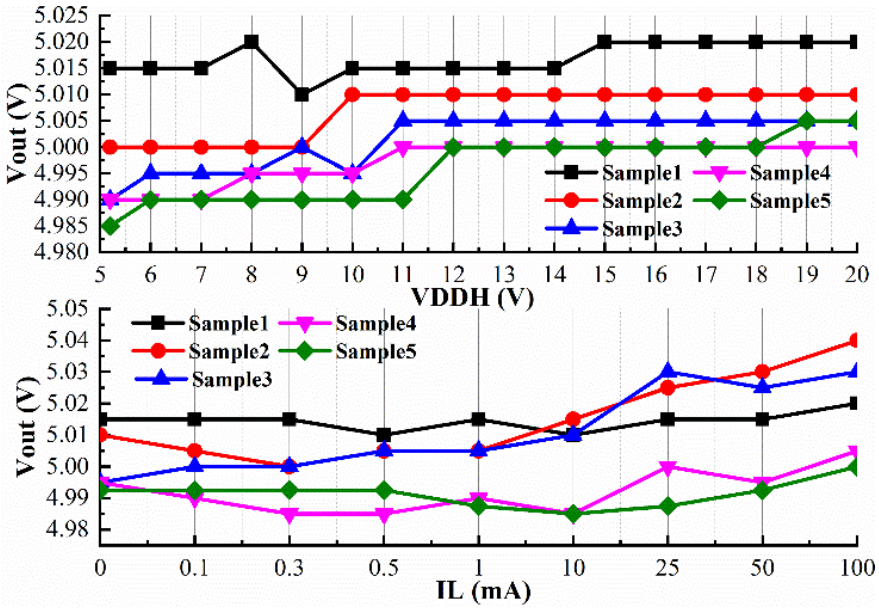

Fig. 5 *Measured line regulation results (I_L=0mA) and load regulation results (VDDH=10V) of five samples.*

Fig. 6 *Transient performance test setup and the measured line transient response at I_L =50mA and C_L =0 pF.*

Fig. 7 *Μεασυρεδ λοαδ τρανσιεντ ρεσπονσε ωιτη ΄΄ΔΔH = 20 ΄΄ (a) ΄΄Λ = 0 πΦ, $T_{Eδγε}$= 1 μς, (β) ΄΄Λ = 100 νΦ, $T_{Eδγε}$= 1 μς, (ς) ΄΄Λ = 22 μΦ, $T_{Eδγε}$= 1 μς.*

and load regulation for 5 samples. I_L =0mA, VDDH varies between 5.2-20 V, the average value of ΔVout is 13 mV, and the line regulation reaches 0.88mV/V. VDDH=10V, I_L varies between 0-100mA, the average value of ΔVout is 22 mV, and the load regulation is 0.22 mV/mA.

Fig. 6 shows the transient performance test setup and the measured line transient response, it can be obtained that this design has a fast line transient response with overshoot/undershoot of 60/20mV under the line-step slew rate of 9.8V/μs.

Fig. 7 presents the load transient response of the proposed HVLDO under different conditions. It can be observed that I_L jumps from 0-100mA with an edge time of T_{Edge} = 1 μs. When the load capacitances C_L of (a), (b) and (c) are 0 pF, 1 nF and 1 μF, respectively, the overshoot /undershoot voltages were 30/70 mV, 30/60 mV and 15/25 mV, respectively. In conclusion, the proposed HVLDO has a fast transient response in the load capacitance range of 0-1 μF.

Table 1. *Comparation with the state-of-the-art*

Parameter	[2], 2019	[3], 2021	[4], 2020	[5], 2014	**This work**
Tech (μm)	0.18	0.4	0.18	0.6	**0.5**
Area (mm^2)	0.18	0.544	0.184	0.3	**0.29**
V_{in} (V)	3.3	4.3-24	5-12	4-40	**5.2-20**
V_{out} (V)	2.8	3.3	4	2.5-5	**5**
Vdo (mV)	500	1000	1000	>200	**200**
TC (ppm/)	NA	185	30	NA	**13.15**
I_{LOAD} (mA)	100	50	50	30	**100**
I_Q (μA)	32	3.2^*	8.2^*	8^*	**243.8**
LNR (mV/V)	5.6	0.56*	0.34	1.38	**0.88**

Parameter	[2], 2019	[3], 2021	[4], 2020	[5], 2014	**This work**
LDR (mV/mA)	0.028	0.26	NA	0.335	**0.22**
LNTR (mV)	65/75	NA	NA	NA	**60/20**
$T_{\text{Edge, LNTR}}$ (µs/V)	10/3-3.5	NA	NA	NA	**1/5.2-15**
LDTR (mV)	170/640	NA	NA	83/103	**30/70**
$T_{\text{Edge, LDTR}}$ (µs/A)	0.1/100m	NA	NA	1/100m	**1/100m**
Setting Time (µs)	52	NA	NA	>10	**2**
PSR (dB) at 100kHz	NA	NA	>-40	NA	**-49**
C_{TOT} (pF)	100	1000	2200	1000	**5**
FOM (fs)	25.92	NA	NA	1653.3	**12.19**

*Minimum value

Table 1 provides a performance comparison with the state-of-the-art. Among all products, the proposed HVLDO has the fastest transient response, short recovery time, lower line regulation and fastest line transient response without off-chip capacitors. The design provides a maximum output current of 100mA and an output voltage of 5V over a wide supply range of 5.2-20V and achieves a temperature coefficient of 13.15 ppm/°C. To compare various regulators implemented in different technologies, an FOM is adopted from [7] and [8]. The smaller the FOM, the better the transient response achieved by the LDO. As shown in Table 1, the proposed HVLDO achieves the smallest FOM factor among all these products.

$$FOM = K * \frac{C_{\text{TOT}} \times V_{\text{out}} \times I_Q}{I_{\text{LOAD}}^2} \# \, (1)$$

$$K = \frac{\Delta t \text{ used in the measurement}}{\text{the maximum } \Delta t \text{ in the design for comparison}} \# \, (2)$$

Conclusions: This work presents a wide input range, external capacitor-Less LDO based on a transient enhancement loop. The proposed HVLDO can provide a regulated 5 V output over an input voltage range of 5.2-20 V with a maximum load of 100 mA, line regulation of 0.88 mV/V, load regulation of 0.22 mV/mA, PM over 68.4 deg and PSR of -49 dB@100 kHz for all load conditions. In particular, the design features fast line transient response of 60/20mV over/undershoot voltage and fast transient response of 30/70mV over/undershoot voltage and 2 µs setting time, which achieves the transient FOM of 12.19 fs. In summary, the proposed HVLDO is suitable for applications in high-voltage power supplies.

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Conflict of interest: No financial interests/personal relationships need to be considered as potential competing interests.

Data availability statement: The data that support the findings of this study are available from the corresponding author upon reasonable request.

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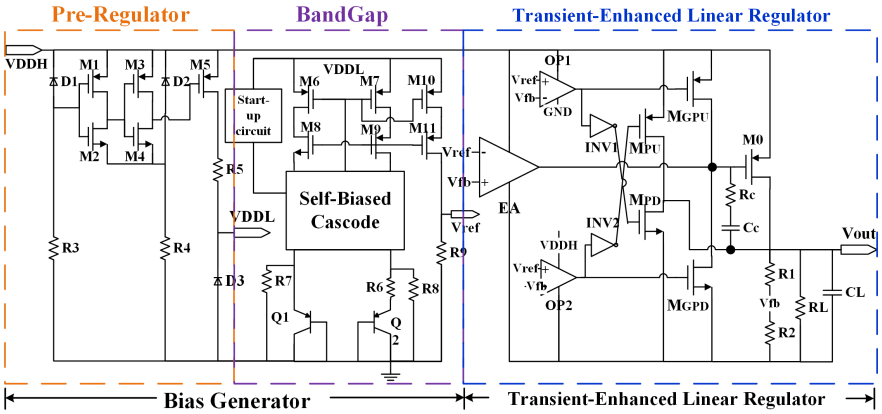

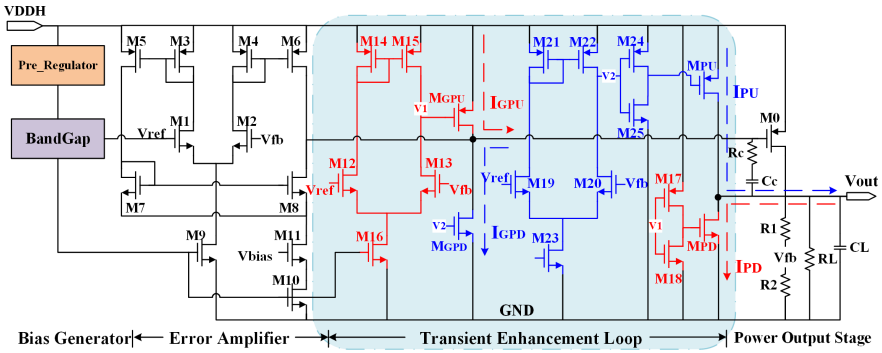

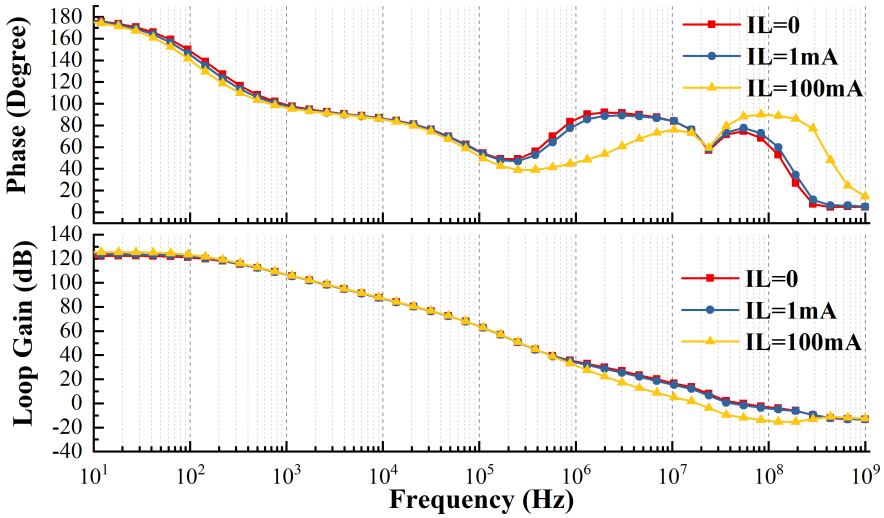

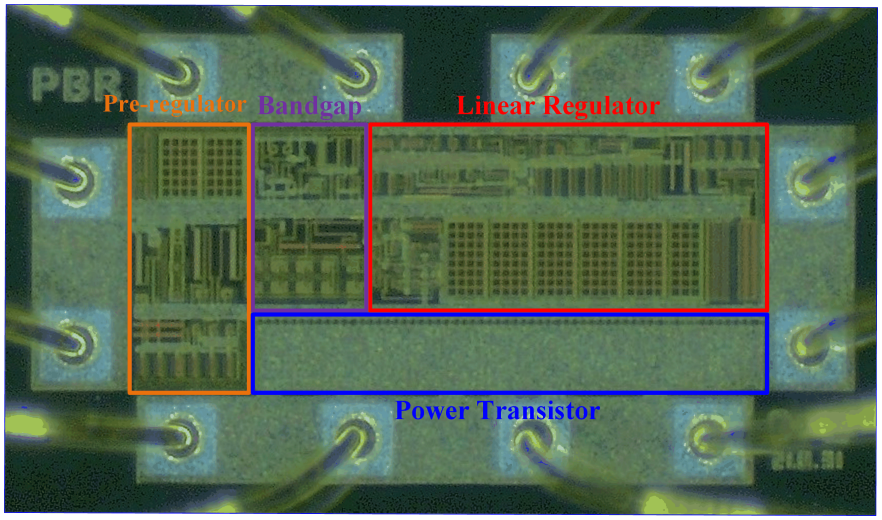

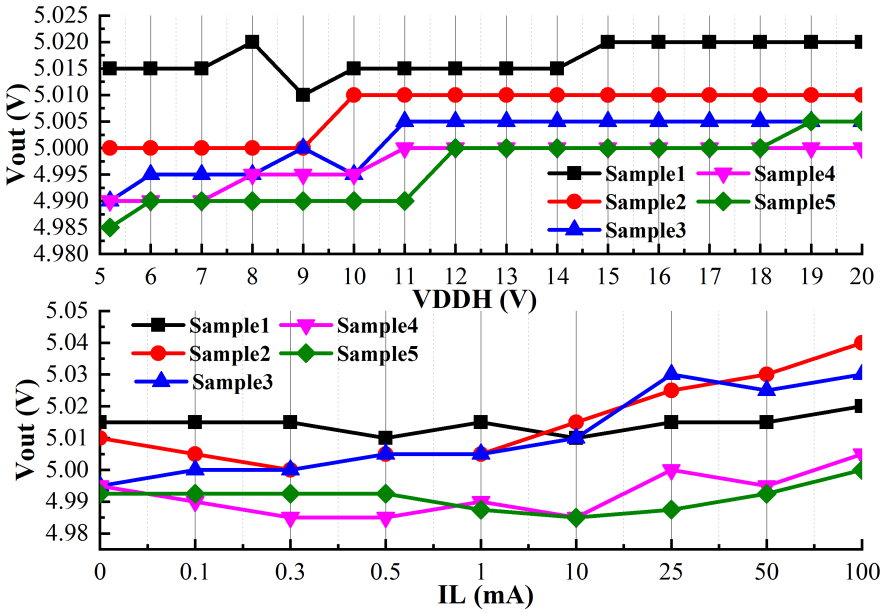

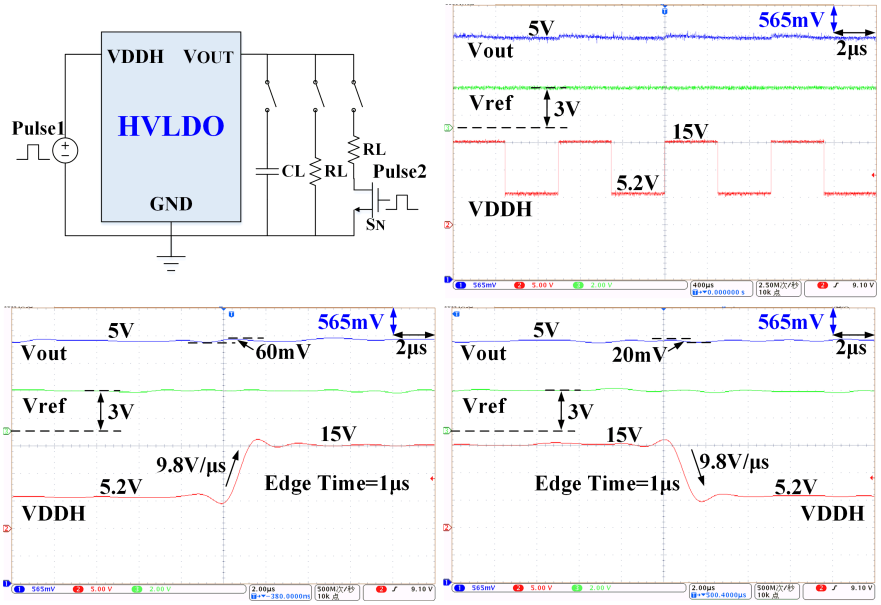

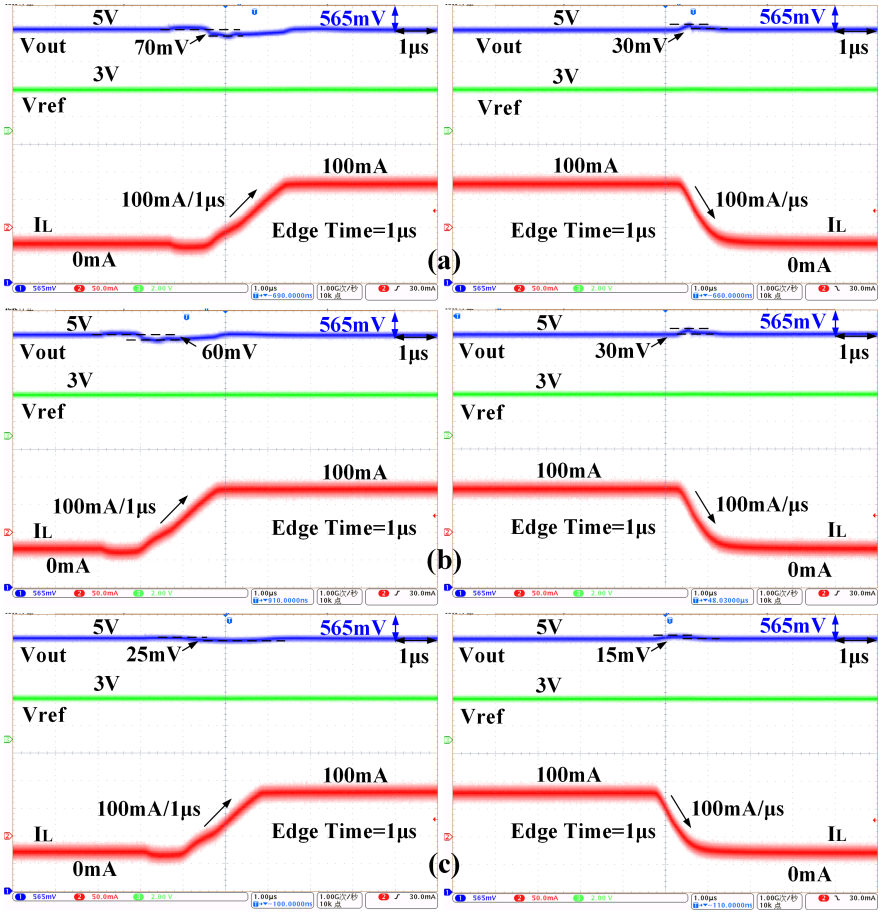

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Table 1. Comparation with the state-of-the-art.docx available at https://authorea.com/users/517127/articles/591773-a-wide-input-range-external-capacitor-less-ldo-with-fast-transient-response