FPGA Realization of an Unsigned Self-Timed 32-Bit Shift-Add Multiplier

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Abstract

Multiplication and addition determine the performance of general and special purpose processors because they are fundamental arithmetic functions. A variety of architectural realizations are needed for these functions to support the range of tradeoffs required for the board class of digital applications. A novel 32-bit unsigned shift-add multiplier Field Programmable Gate Array (FPGA) realization is proposed in this letter that has a performance-energy dissipation metric sufficiently different from previously proposed architectures that potentially permit new applications. The number of clock cycles required to complete the multiplication equals the number of 0s and 1s substrings in the multiplier operand. The multiplier is faster than an array multiplier if the multiplier operand contains less than 10 0s and 1s substrings. It is fast than the carry-save array multiplier if the number of 0s and 1s substrings in the multiplier operand is five or fewer. Requires approximately the same resources as an array multiplier and less than half the resources required for a carry-save array multiplier.

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