Threshold voltage instability and device failure mechanism of p-GaN gate HEMTs under repetitive short-circuit stress

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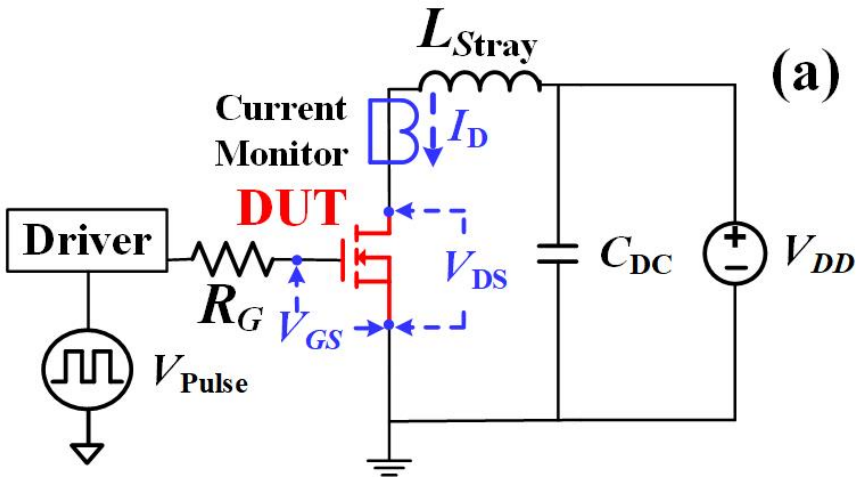
Abstract

In this letter, the underlying physics of threshold voltage (Vth) instability and the eventual device failure mechanism of 100V Schottky p-GaN gate high electron mobility transistors (HEMTs) under repetitive short-circuit (SC) stress with varied drain voltage (VDD= 40-70V) and SC pulse duration (TSC=10 μs & 20 μs) is studied. In the lenient SC stress with lower SC energy (e.g. SC stress @ VGS=6 V, VDD=40-70 V, TSC=10 μs), the devices exhibit significantly positive Vth shift while the Vth instability shows positive dependence with the stressed drain voltage and the repetitive SC pulses. For device stressed at VDD=70 V with 150 SC pulses, a substantial ΔVth as high as +0.68 V is observed. Such a prominent Vth instability is induced by the electron trapping in the p-GaN gate region during the SC events, which also results in the suppressed gate and drain leakage current after SC stress. In the more stringent SC stress (VGS=6 V, VDD=70 V, TSC=20 μs) with much higher corresponding SC energy, the device failed due to the drain electrode burned out initiated by the significantly high SC energy during the SC events.



Threshold voltage instability and device failure mechanism of p-GaN gate HEMTs under repetitive short-circuit stress

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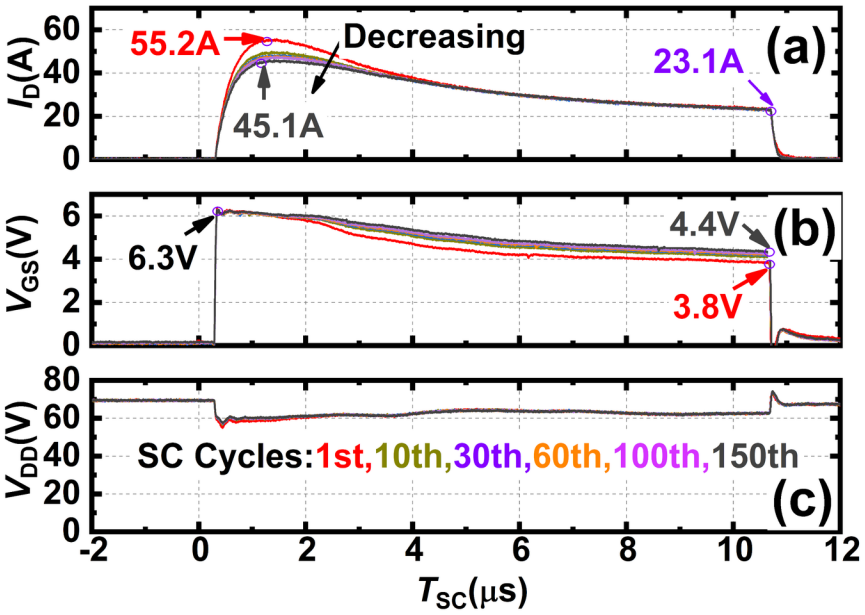

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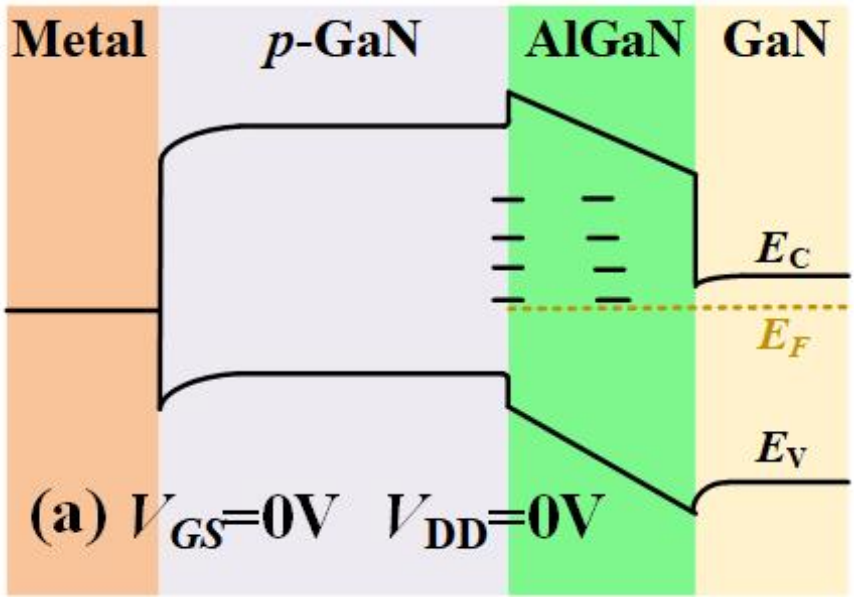
In this letter, the underlying physics of threshold voltage ($V_{\rm th}$) instability and the eventual device failure mechanism of 100V Schottky p-GaN gate high electron mobility transistors (HEMTs) under repetitive short-circuit (SC) stress with varied drain voltage ($V_{\rm DD}$= 40-70V) and SC pulse duration ($T_{\rm SC}$=10 μs & 20 μs) is studied. In the lenient SC stress with lower SC energy (e.g. SC stress @$V_{\rm GS}$=6 V, $V_{\rm DD}$=40-70 V,$T_{\rm SC}$=10 μs), the devices exhibit significantly positive $V_{\rm th}$ shift while the$V_{\rm th}$ instability shows positive dependence with the stressed drain voltage and the repetitive SC pulses. For device stressed at $V_{\rm DD}$=70 V with 150 SC pulses, a substantial $\Delta V_{\rm th}$ as high as +0.68 V is observed. Such a prominent $V_{\rm th}$ instability is induced by the electron trapping in the p-GaN gate region during the SC events, which also results in the suppressed gate and drain leakage current after SC stress. In the more stringent SC stress ($V_{\rm GS}$=6 V, $V_{\rm DD}$=70 V,$T_{\rm SC}$=20 μs) with much higher corresponding SC energy, the device failed due to the drain electrode burned out initiated by the significantly high SC energy during the SC events.

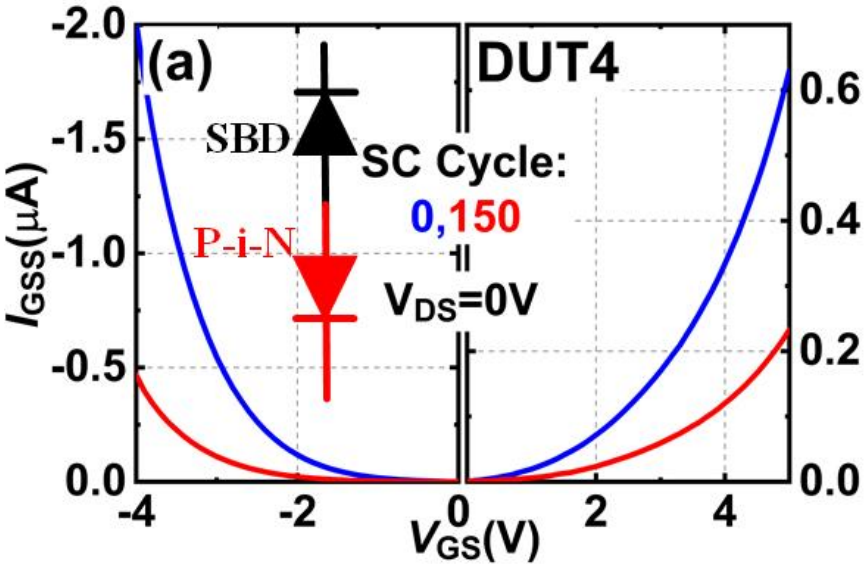
Introduction: In recent years, owing to its superior power performance, the p-GaN gate HEMTs have been commercialized and used in fast charger, LiDAR, and data-center *etc* . However, the device stability is still a challenge and the underlying physics responsible for the device instability as well as the device failure mechanism are of great interests for further improvement of the device stability to deliver stable and high-power performance of GaN power electronics. In the high frequency power applications, such as PFC converter and LLC resonant circuit, short circuit (SC) robustness is important for the stable and safe operation of power circuits. The SC fault may occur due to the failure or short in the load, faulty gate control signals, crosstalk in a phase-leg circuit [1], [2] *etc* . During the SC events, the device simultaneously undergoes a high bus voltage and large SC current, such a harsh condition may result in significant device degeneration or even destructive failure, which is one of the biggest impediments for the safe and efficient operation of GaN power conversion systems. Hence, investigating the device instability and failure mechanism is of great importance to improve the SC stability of p-GaN gate HEMTs.

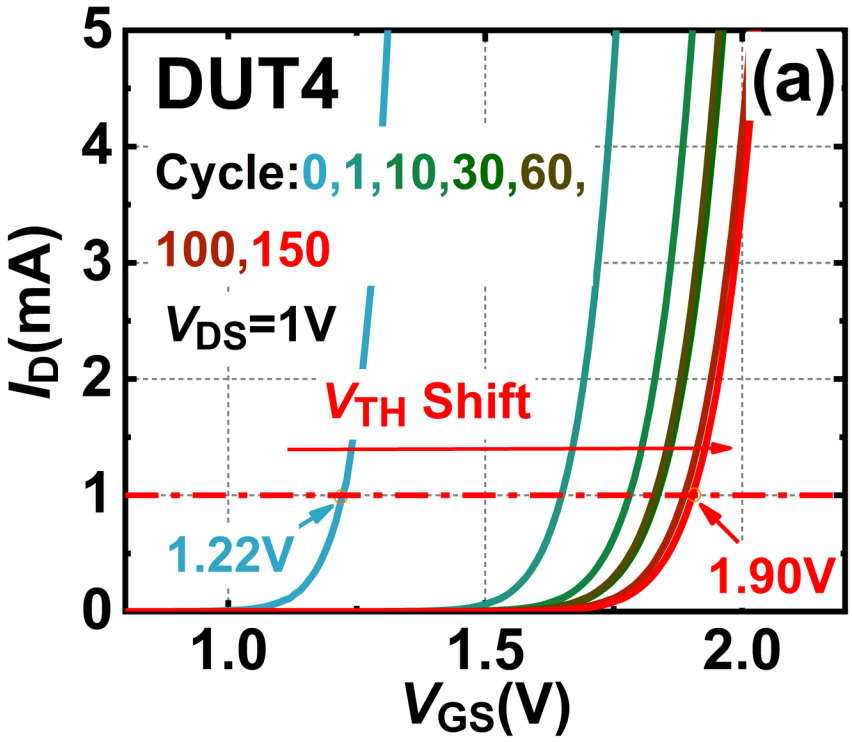
Recently, the SC characteristics of 600V/650V high voltage p-GaN gate HEMTs under different SC conditions have been investigated [3]-[6]. The high voltage HEMTs exhibit weak repetitive SC capability since the high SC energy generates significant heat during the SC events which leads to prominent mechanical stress and

then results in fatigue or fracture failure [4]. However, the SC characteristics and device instability of 100 V low-voltage p-GaN gate HEMTs are rarely reported [7]. Particularly, the ultimate device failure mechanism under SC events is still lacking up to date.

In this work, by conducting the repetitive SC stress with up to 150 pulse cycles and varied stress V_{DD} and T_{SC}, the V_{th} instability during the evolution of the SC stress is recorded and the underlying mechanism is studied. By further enhancing the stress condition with higher SC energy, the eventual device failure is observed and the failure mechanism is revealed by studying the SC waveform and chip microscopy. The experimental results show that the studied 100 V p-GaN gate HEMTs feature quite different SC characteristics from the reported 600/650 V p-GaN gate HEMTs [3]-[6].



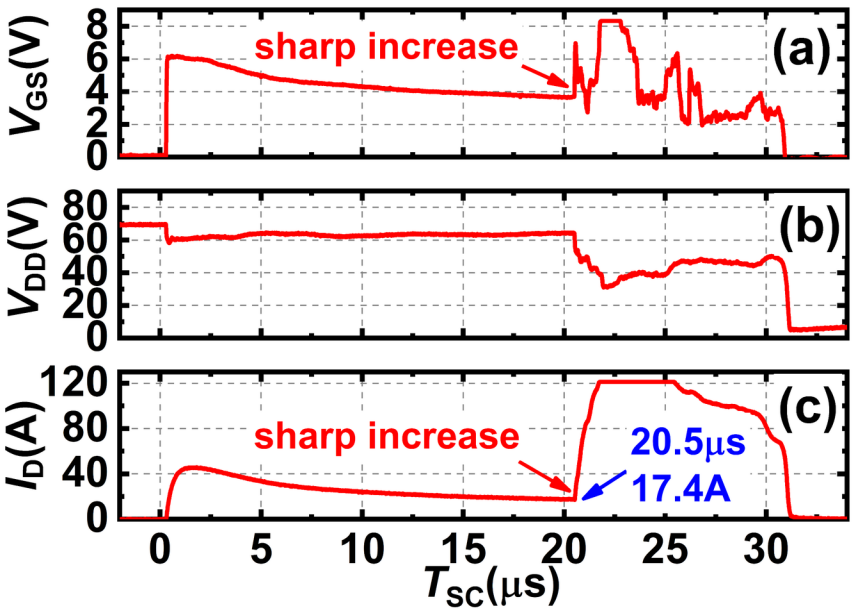




Experiments and discussion: The device studied is the 100 V/25 mΩ Schottky-type p-GaN gate HEMTs commercial product. The device structure can be found in our previous report [7]. Fig. 1 (a) plots the SC measurement circuit. Fig.1 (b) shows the repetitive SC stress and device characterization strategy. The devices were stressed by up to 150 SC pulses that is 50% higher than our previous report [7], while the device characteristics were respectively recorded after the 1^{st}, 10^{th}, 30^{th}, 60^{th}, 100^{th} , and 150^{th} SC pulse during the repetitive SC evolution. Fig. 2 plots the typical repetitive SC waveforms of V_{GS}=6 V, V_{DD}=70 V and T_{SC}=10 μs for the 1^{st} , 10^{th} , 30^{th} , 60^{th} , 100^{th} , and 150^{th} SC cycle. Within each SC event, the decreased SC drain current I_D is a result of the significantly high SC current induced junction temperature T_j increase [4] and the subsequent 2DEG mobility reduction [8]. In addition, the peak SC I_D reduced from 55.2 to 45.1 A due to the positive shift of V_{th}. Besides, the increased T_j may also result in gate leakage increase during the SC event [7], which leads to a higher voltage drop across the resistor (R_G) connected to the gate terminal as shown in Fig. 1 (a). As a result, the SC waveform of V_{GS} exhibits a moderate decrease within a single SC event as can be seen in Fig. 2 (b). On the other hand, together with the evolution of the repetitive SC cycles, the consistent trap filling in the gate region results in suppressed gate leakage which leads to a reduced voltage across R_G and then a higher effective gate bias is applied at the gate terminal of the device. Hence, the V_{GS} at the end point of the V_{GS} SC waveform exhibits a marginal increase (see Fig. 2 (b)). The repetitive SC experiments are conducted on DUT1, 2, 3 and 4 at V_{GS} =6 V, T_{SC}=10 μs, and varied V_{DD}=40 V, 50 V, 60 V and 70 V, respectively. Fig.3 (a) shows the transfer curves of DUT4. It can be seen that the transfer characteristic exhibits a substantial positive shift which leads to the V_{th} (defined at I_{DS}=1 mA) significantly shifted from 1.22 V in the fresh device to 1.90 V after SC stress. Fig. 3 (b) plots the ΔV_{th} of DUT 1˜4 versus the SC cycles. The ΔV_{th} increases with the increasing SC cycles and gradually saturates for SC cycles >120. Moreover, with the identical SC stress cycles, the device exhibits higher ΔV_{th} stressed with higher V_{DD}. Even though exhibiting substantial V_{th} instability, all of the 4 tested devices were not failed after 150 SC cycles that suggests the strong repetitive SC capability of the devices, which is quite different from the reported 650 V Schottky p-GaN gate HEMTs featuring weak repetitive SC capability [4]. However, it should be pointed out that the significantly positive V_{TH} shift

may induce an insufficient turn-on of GaN HEMTs as well as additional turn-on loss, which is detrimental to achieve high power efficiency of GaN HEMTs particularly for the low voltage GaN HEMTs that is supposed to operate at higher frequency where the switching loss is crucial for the power circuits.

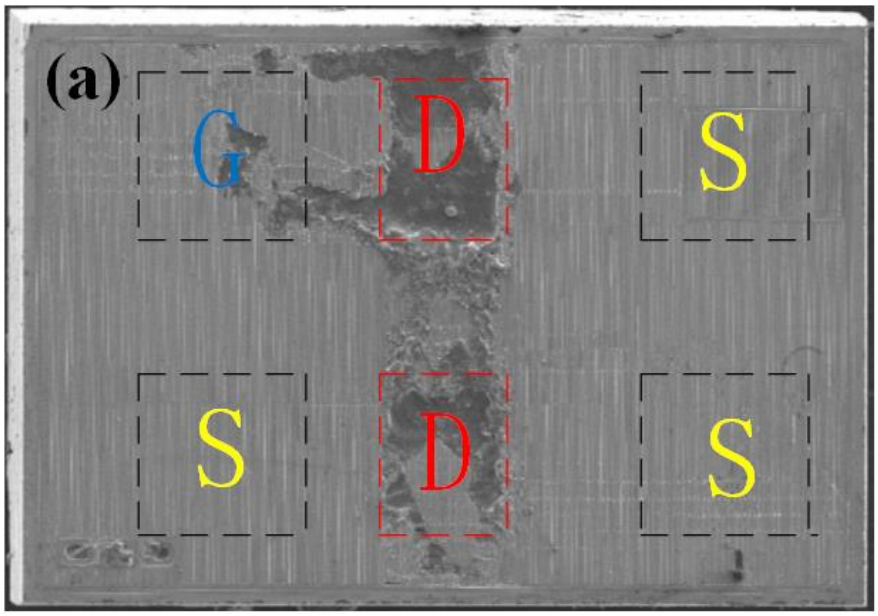
Fig.4 compares the typical gate leakage current I_{GSS} and off-state drain leakage current I_{DSS} of DUT-4 before and after SC stress. I_{GSS} is measured with source/drain terminal grounded, while I_{DSS} is measured in off-state with V_{GS}=0 V. In positive gate bias, the applied voltage mainly drops across the upper metal/p-GaN Schottky diode in reverse mode, which facilitates blocking the gate leakage. In contrast, in negative gate bias, the upper Schottky diode is biased in forward mode that enables hole current conduction. Meanwhile, the applied gate voltage mainly drops across the p-i-n diode in reverse mode, which leads to higher reverse leakage by trap-state assistant electron tunneling due to the presence of trap states at p-GaN/AlGaN interface (e.g. N-vacancy or Ga-dangling bond) [9], [13] and in AlGaN barrier induced by Mg-dopant out-diffusion [10], [12]. Hence, the overall reverse gate leakage is higher than that in forward. Moreover, it can be seen that the I_{GSS} exhibits a reduction after SC stress. Because the positive gate bias during the SC stress can sufficiently lower the p-GaN/AlGaN barrier, the significantly high SC current flows through the device with a large amount of 2DEG accumulated at the AlGaN/GaN interface channel. Meanwhile, the respectable large potential difference between gate and drain during SC event may result in a high electric-field located at the drain-side gate edge [4]. In this manner, driven by the locally high electric-field part of the high-density electrons in the channel can leap over the lowered energy barrier or tunneling through p-GaN/AlGaN gate stack, which leads to the increased gate leakage during the SC event and the simultaneous electron trapping by interface states at the p-GaN/AlGaN interface [11] and bulk traps in AlGaN barrier as depicted in Fig. 5. After occurrence of the electron-trapping, the interface states and bulk states filled with electrons are negatively charged, which tends to deplete the 2DEG in the channel and then results in positive shift in V_{th}. The trap states are gradually filled along with the increasing SC cycles. Hence, the ΔV_{th}increases with the SC cycles and then exhibits a saturation trend as observed in Fig. 3. Besides, the negatively charged traps can effectively suppress the gate leakage after stress as observed in Fig. 4 (a). Fig. 4 (b) shows the drain leakage I_{DSS} and gate leakage I_G in off-state measured before and after SC stress of DUT4. The identical I_{DSS} andI_G suggests that the off-state leakage of the device is dominated by the drain-to-gate leakage. More importantly, similar to I_{GSS} measured in Fig 4(a), the off-state I_{DSS} as well asI_G show an obvious reduction after SC stress as shown in Fig. 4 (b), which reinforces that the occurrence of electron trapping in the p-GaN gate stack rather than in GaN buffer beneath the 2DEG channel.



As the devices (i.e. DUT1˜4) were not failed, more stringent stress was further used to investigate the device failure mechanism. The DUT5 was stressed at V_{GS}=6 V, V_{DD}=70 V with a larger SC pulse duration of T_{SC}=20 µs. DUT5 failed within the 16^{th} SC cycle with the SC waveform as shown in Fig. 7. It can be seen that the SC current I_D exhibits an abrupt increase at 20.5 µs. The failed device behaves as the typical electrical shorting behavior between the drain and gate terminal. The failed device is then decapsulated and drain electrode burnout was observed in Fig. 8 (a). Since the SC current before the device failure is 17.4 A that is even lower than that as shown in Fig. 2 (b), the device failure is prone to be induced by the substantially high SC energy and its accumulation effect during the repetitive SC events (e.g. the 1^{st} ˜15^{th} SC cycles) prior to eventual device failure.

We compare the SC energy (E_{SC}) of a single SC pulse of DUT-1˜5 as illustrated in Fig. 8 (b). It is worth noticing that E_{SC} increases with the enhanced SC stress. Besides, the E_{SC} of DUT1-4 are much lower compared with DUT-5 attributes to the longer T_{SC}. More importantly, the much higher SC energy can cause a higher local temperature close to the drain electrode [3], [4]. The local temperature fluctuates between on-state and off-state in the repetitive SC cycles, generating cyclic mechanical stress of thermal expansion and contraction phases. Together with the repetitive SC events, the mechanical stress leads to accumulative degradation at drain electrodes during the 1^{st} to 15^{th} SC cycles. After that, in the 16^{th} SC cycle, the accumulative degradation exceeds to a critical level and leads to fatigue failure and then the subsequent gate-to-drain short circuit with abrupt increase in SC I_D as observed in Fig. 7(c). Consequently, the substantially high current results in the catastrophic thermal burned up of the two drain electrodes as shown in Fig. 8 (a).

Conclusion: The SC capability and device failure mechanism of the 100 V p-GaN gate HEMTs were investigated by the repetitive SC stress. In the repetitive SC stress with 150 SC cycles at V_{GS}=6 V, V_{DD}=40˜70 V and T_{SC}=10 µs, the device exhibits strong repetitive SC capability without device failure. However, significant positive shift in V_{th} stems from electron trapping in the p-GaN/AlGaN gate stack is observed prior to the device failure. Accordingly, the electron-filled traps in turn to result in a suppressed gate leakage and off-state drain leakage current in the device after SC stress. By further enhancing the SC stress condition with a larger SC duration of 20 µs, the device can withstand ˜15 cycles at V_{GS}=6 V and V_{DD}=70 V. The resultant significantly higher SC energy leads to thermal fatigue crack formation at the drain electrode due to the local temperature fluctuations, which results in the consequent thermal burnout.



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