High-Performance In0.53Ga0.47As/InAs/In0.53Ga0.47As Composite Channel Metamorphic HEMTs (MHEMTs) on GaAs Substrate

Seung Heon Shin[1], Jae-Phil Shim[2], Hyunchul Jang[2], and Jae-Hyung Jang[3]

[1]Korea Polytechnics
[2]Korea Advanced Nano Fab Center
[3]Korea Institute of Energy Technology

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Abstract

In this work, we successfully demonstrated In0.53Ga0.47As/InAs/In0.53Ga0.47As composite channel metamorphic high electron mobility transistors (MHEMTs) on GaAs substrate for the first time. The fabricated MHEMTs with 100 nm gate length exhibited excellent DC and logic characteristics such as VT = -0.13V, gm,max = 949 mS/mm, subthreshold swing (SS) = 84 mV/dec, drain-induced barrier lowering (DIBL) = 89mV/V, and Ion/Ioff ratio = 9.8 X 103 at VDS = 0.5 V. In addition, the device exhibited excellent high frequency characteristics such as fT/fmax = 261/304 GHz at VDS = 0.5 V and these high frequency characteristics is the well-balanced demonstration of fT and fmax in the MHEMT structure on GaAs substrate.

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In this work, we successfully demonstrated $In_{0.53}Ga_{0.47}As/InAs/In_{0.53}Ga_{0.47}As$ composite channel metamorphic high electron mobility transistors (MHEMTs) on GaAs substrate for the first time. The fabricated MHEMTs with 100 nm gate length exhibited excellent DC and logic characteristics such as V_T = -0.13V, $g_{m,max}$ = 949 mS/mm, subthreshold swing (SS) = 84 mV/dec, drain-induced barrier lowering (DIBL) = 89mV/V, and I_{on}/I_{off} ratio = 9.8 X 10^3 at V_{DS} = 0.5 V. In addition, the device exhibited excellent high frequency characteristics such as f_T/f_{max} = 261/304 GHz at V_{DS} = 0.5 V and these high frequency characteristics is the well-balanced demonstration of f_T and f_{max} in the MHEMT structure on GaAs substrate.

Introduction: High electron mobility transistors (HEMTs) based on Indium-rich $In_xGa_{1-x}As$ channel materials on InP substrate has demonstrated excellent high frequency and logic characteristics. H. -B. Jo et al. demonstrated 738 GHz unity current gain cutoff frequency (f_T) in 19 nm $In_{0.8}Ga_{0.2}As$ composite-channel HEMT on InP substrate [1] and D. -H. Kim et al. showed excellent logic performance and f_T of 644 GHz in 30 nm InAs Pseudomorphic HEMTs (PHEMTs) [2]. These remarkable performances have been achieved by using downscaling of feature size and the optimized InGaAs channel materials for excellent transport properties. However, large size substrate will be essential for large volume manufacturing, but InP substrate size is limited to 4-inch up to now. To overcome size limitations, many groups have demonstrated many outstanding results of MHEMTs on GaAs substrate [3-6]. Especially, D.-H. Kim of Teledyne demonstrated excellent results of 688 GHz f_T by utilizing $In_{0.7}GaAs$ MHEMT structure on GaAs substrate in 2011 [4] and A. Leuther of Fraunhofer showed f_{max}exceeding 1000 GHz by using $In_{0.8}GaAs$ MHEMT structure on GaAs substrate in 2013 [6]. Among various HEMT structures, InGaAs/InAs/InGaAs composite channel was

used to enhance high-frequency characteristics in p-HEMT structures because of excellent electron transport properties such as electron velocity and electron mobility [2, 7] but $In_{0.53}Ga_{0.47}As/InAs/In_{0.53}Ga_{0.47}As$ composite channel structure on GaAs substrate have not been demonstrated. In this work, we investigated performances of the MHEMT on GaAs substrate by utilizing $In_{0.53}Ga_{0.47}As/InAs/In_{0.53}Ga_{0.47}As$ composite channel HEMT structure for the first time.

Layer structure and experiments: The MHEMT heterostructures consisted of a 500 nm $In_{0.52}Al_{0.48}As$ buffer, a 12 nm $In_{0.53}Ga_{0.47}As/InAs/In_{0.53}Ga_{0.47}As$ (4/5/3 nm) channel, a 3 nm $In_{0.52}Al_{0.48}As$ spacer, a Si δ-doping (4.1 X 10^{12} cm^{-2}), an 8 nm $In_{0.52}Al_{0.48}As$ barrier, a 4 nm InP etch stop layer, and a 35 nm heavily doped $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ multi-layer cap from bottom to the top. This structure showed sheet carrier density and electron hall mobility were 2.92 x 10^{12} cm^{-2} and 10,000 $cm^2/V{\cdot}S$.

Device fabrication began with 30nm Molybdenum (Mo) deposition for ohmic contact to prevent surface contamination and mesa isolation down to an InAlAs buffer layer by Mo dry etching and wet etching. After Ti/Au/Ni (20/150/30 nm) metallization for source and drain, dry etching in an SF_6/Ar plasma was performed to etch Mo in the gate region [8]. The ohmic contact resistance (R_c) measured by the TLM (transmission line method) was as low as 0.01 Ω*mm. A 30 nm-thick SiO_2 was deposited by plasma enhanced chemical vapor deposition (PECVD) and then, the pad patterns with Ti/Au (20/300 nm) were defined for ground-signal-ground probing. After e-beam exposure, the defined e-beam resist pattern was transferred to define T-gate by using reactive ion etching based on CF_4plasma. Gate recess was performed in two different step stages and then, anisotropic reactive ion etching of the InP etch stop layer in an Ar-based plasma [9]. After InP etching, Schottky gate metallization of Ti/Pt/Au (20/30/300 nm) was deposited on top of the InAlAs layer.

Result and discussion: The transfer characteristic and output characteristics of the MHEMTs are shown in Fig 1. The maximum transconductance ($g_{m,max}$) and maximum drain current density ($I_{D,max}$) were 949 mS/mm and 413 mA/mm at V_{DS} = 0.5V, respectively. The output characteristics presented in Fig 1 (inset) show good pinch-off characteristics but measured R_{on} was 733 Ω-um, which is a higher value than the lift-off Mo/Ti/Mo/Au metal scheme [10] because of SF_6/Ar plasma damage in the active region during Mo etch to define gate active region. Fig 2 shows the subthreshold characteristics at V_{DS} = 0.5 V and 0.05 V, respectively. At V_{DS} = 0.5 V, the threshold voltage (V_T) is -0.13 V which was defined as the value of V_{GS} that yields at I_D = 1 mA/mm and the device shows excellent electrostatic integrity such as the subthreshold swing (SS) is 84 mV/dec, the drain induced-barrier lowering (DIBL) is 89 mV/V, and I_{on}/I_{off} ratio is 9.8 X 10^3 respectively. These outstanding logic performances are because of the well-designed heterostructure on GaAs substrate and optimized process conditions.

Fig. 1 *Transfer characteristics of the MHEMT at V_{DS} = 0.5 V. (Inset) Output characteristics of the MHEMT (V_{GS} = -0.5 V ˜ 0.5V).*

Fig. 2 *Subthreshold characteristics of the MHEMT measured at V_{DS} = 0.5 V and V_{DS} = 0.05 V, respectively.*

To verify the high-frequency RF characteristics of the MHEMT, S-parameters were measured from 0.5 GHz to 40 GHz by using a vector network analyzer. The de-embedding method used open and short patterns to extract parasitic pad capacitance and inductance. Fig 3 shows unity current gain cutoff frequency (f_T), maximum oscillation frequency (f_{max}), maximum stable gain (MSG)/maximum available gain (MAG), and stability factor (K) against frequency for the best condition at V_{DS} = 0.5 V and V_{GS} = 0.2 V with L_g = 100 nm MHEMT device. Values of f_T = 261 GHz and f_{max} = 304 GHz have been shown by extrapolation. Fig 4 shows f_T and f_{max} as a function of I_{DS} at V_{DS} = 0.5 V and 0.4 V. Around I_{DS} of 75 mA/mm, our device already demonstrated f_T and f_{max} over 200 GHz.

Table. 1 benchmark high-frequency characteristics and structures for the MHEMT fabricated in this paper on GaAs substrate compared to published state-of-the-art MHEMT research results. We obtain excellent $L_g f_T$ of 26.1 GHz-um, which is related to excellent carrier transport properties [11], and the f_T/f_{max} of 261/304 GHz with 100 nm gate length at lower V_{DS} = 0.5 V compared to other structures. These excellent performances are mainly attributed to well-grown $In_{0.53}Ga_{0.47}As/InAs/In_{0.53}Ga_{0.47}As$ composite channel

structure on GaAs substrate.

Fig. 3 *Maximum oscillation frequency (f_{max}), maximum stable gain (MSG)/maximum available gain (MAG), stability factor (K), and unity current gain cutoff frequency (f_T) of the MHEMTs at V_{DS} = 0.5 V and V_{GS} = 0.2 V.*

Fig. 4 *Maximum oscillation frequency (f_{max})* and unity current gain cutoff frequency (f_T) of the *MHEMTs against drain current density at* V_{DS}=0.5 and 0.4 V, respectively.

Table 1 Performance parameters of the MHEMTs on GaAs substrate.

	[12]	[4]	[6]	[13]	**This work**
Channel	$In_{0.8}GaAs$	$In_{0.7}Ga_{0.3}As$	$In_{0.8}GaAs$	$In_{0.6}Ga_{0.4}As$	**$In_{0.53}Ga_{0.47}As$ /InAs/ $In_{0.53}Ga_{0.47}As$**
Buffer layer	1 μm InAlGaAs	0.3 μm graded buffer	1.1 μm InAlGaAs	Graded InAlAs	**500 nm $In_{0.52}AlAs$**
L_g [nm]	20	40	35	100	**100**
f_T [GHz]	660	688	515	210	**261**
f_{max} [GHz]	-	800	> 1000	252	**304**
L_gf_T [GHz-μm]	13.2	27.5	18.0	21.0	**26.1**
V_{DS} [V]	1	0.6	-	1	**0.5**

Conclusion: The 100 nm $In_{0.53}Ga_{0.47}As$/InAs/$In_{0.53}Ga_{0.47}As$ composite channel metamorphic high electron mobility transistors (MHEMTs) by using $In_{0.52}Al_{0.48}As$ buffer layer on GaAs substrate exhibited excellent logic characteristics as well as high-frequency RF performances. These outstanding performances are because of excellent carrier transport properties of well-grown $In_{0.53}Ga_{0.47}As$/InAs/$In_{0.53}Ga_{0.47}As$ composite channel MHEMT structure on GaAs substrate and optimized fabrication process. The proposed MHEMT structure on GaAs substrate together with optimized source/drain and gate technology will have the potential to improve logic and high-frequency characteristics. Furthermore, the proposed MHEMT structure in this work on large-size GaAs substrate will be indispensable for large-volume manufacturing.

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Seung Heon Shin (*Department of Semiconductor Process Equipment, Semiconductor Convergence Campus, Korea Polytechnics, 41-12, Songwon-gil, Gongdo-eup, Anseong-si, 17550, Republic of Korea)*

Jae-Phil Shim and Hyunchul Jang *(Convergence Technology Lab, Korea Advanced Nano Fab Center (KANC), 109, Gwanggyo-ro, Yeongtong-gu, Suwon-si, Gyeonggi-do, 16229, Republic of Korea)*

Jae-Hyung Jang *(Korea Institute of Energy Technology, 200, Hyeoksin-ro, Naju-si, Jellanam-do, 58330, Republic of Korea)*

Seung Heon Shin and Jae-Hyung Jang (Corresponding authors, E-mail:*shshin@kopo.ac.kr,jjang@kentech.ac.kr*)

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