A passive noise-shaping SAR ADC with energy-efficient switching method

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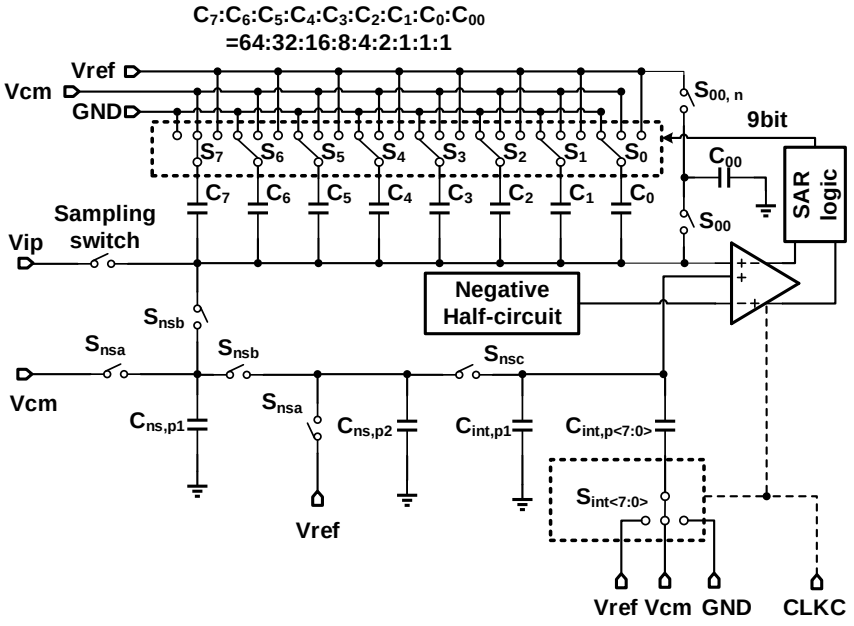
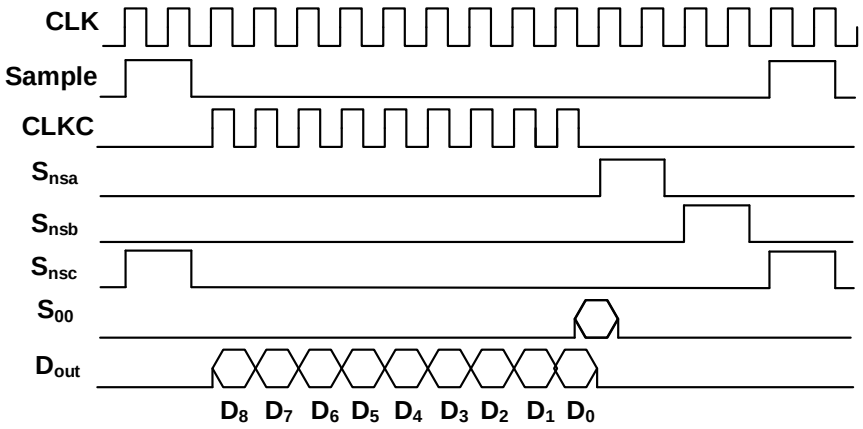
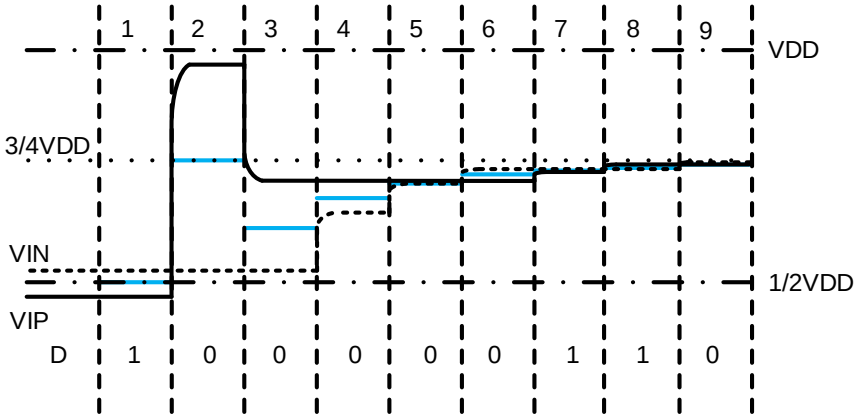
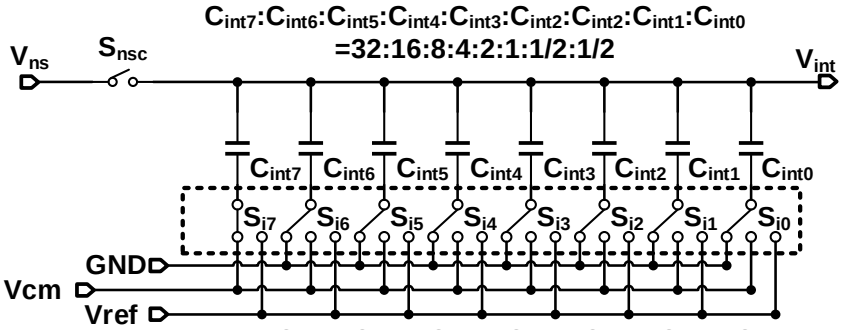
Abstract

In this letter, a low-voltage passive first-order noise shaping charge-redistribution successive approximation register (SAR) ADC with energy-efficient switching method is proposed. The energy-efficient switching method is achieved by one-side switching instead (OSSI) method and higher-bit switching instead (HBSI) method. The architecture is modified to realize the noise-shaping loop properly. We present a passive integrator with a dynamic DC offset to address the path gain error from the varying voltage on the capacitor array at each quantization step. Simulation results on a 180nm CMOS technology operated at 0.6V supply and 25kHz sampling rate show 130nW power consumption with a peak SNDR of 70.3dB.









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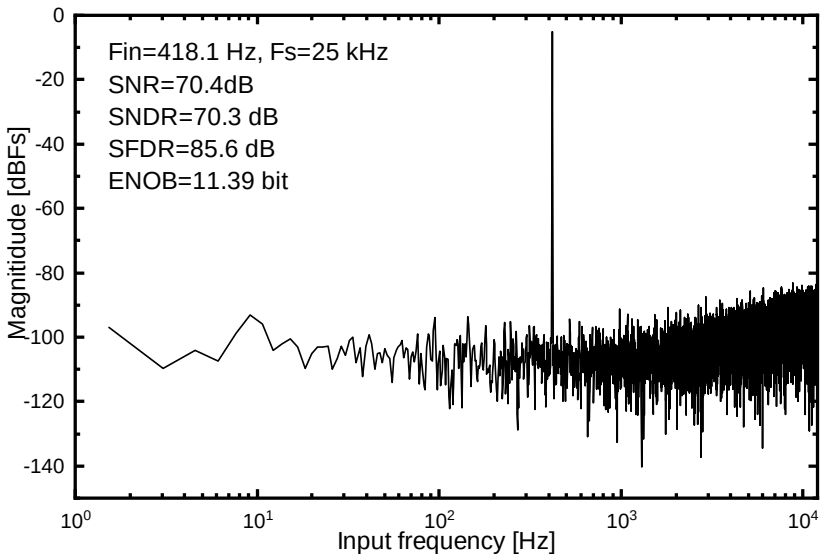

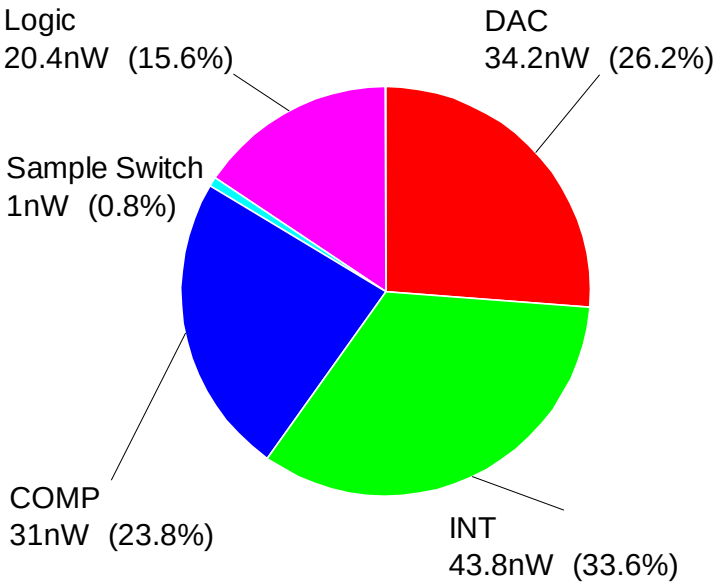

A passive noise-shaping SAR ADC with energy-efficient switching method

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In this letter, a low-voltage passive first-order noise shaping charge-redistribution successive approximation register (SAR) ADC with energy-efficient switching method is proposed. The energy-efficient switching method is achieved by one-side switching instead (OSSI) method and higher-bit switching instead (HBSI) method. The architecture is modified to realize the noise-shaping loop properly. We present a passive integrator with a dynamic DC offset to address the path gain error from the varying voltage on the capacitor array at each quantization step. Simulation results on a 180nm CMOS technology operated at 0.6V supply and 25kHz sampling rate show 130nW power consumption with a peak SNDR of 70.3dB.

Introduction: Low-voltage charge-redistribution successive approximation register (SAR) ADC is a popular architecture for low-power applications. The main part of the power consumption of SAR ADCs is capacitor arrays [1]. To decrease the energy consumption of SAR ADCs, many researchers focus on energy-efficient switching methods in the capacitor arrays. Many switching methods have been proposed to save switching power during the DAC transition. In Ref[2], the authors add a reference voltage at the middle of Vrefp and Vrefn, and realize charge-recovery during each transition bit. Ref [1] proposed a V_{CM} based monotonic switching procedure, which reduces both the switching energy and the number of capacitors. In Ref [3], the first three comparisons with zero energy consumption by adopting one-side switching instead (OSSI) method and higher-bit switching instead (HBSI) method. In addition, we can decrease the total number of capacitor array cells to save more power under the same resolution requirements. Recently, the noise-shaping technique has been applied to high-resolution SAR ADCs by adding a feedback path to avoid using a large input capacitor array [4].

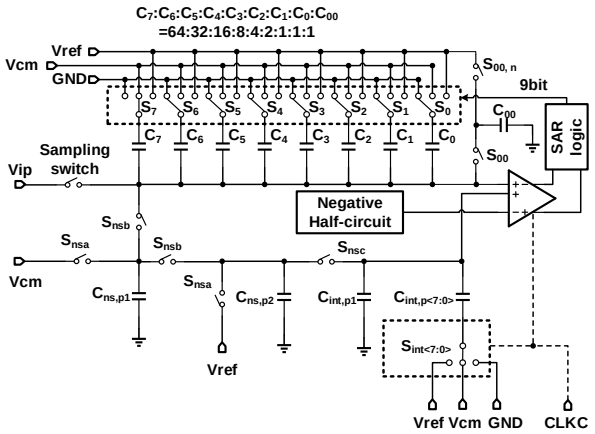

Fig. 1 *Proposed noise-shaping SAR ADC with energy-efficient switching method*

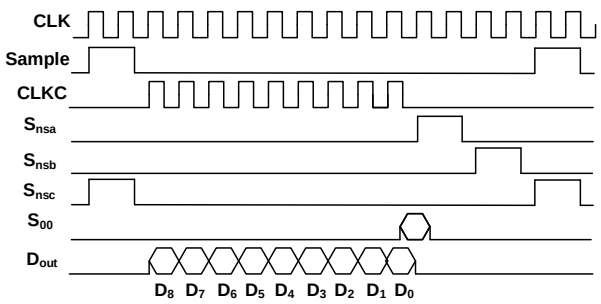

Fig. 2. Timing diagram of proposed noise-shaping SAR ADC

noise-shaping SAR ADC with energy-efficient switching method: In this paper, a new noise-shaping SAR ADC with OSSI method and HBSI method is proposed, which is shown in Fig. 1. It consists of a 9-bit SAR-ADC to realize voltage quantization and a 1-st order passive filter to construct the noise-shaping architecture. Since the energy-efficient switching method is utilized, during the first three comparator cycles, no switching energy is consumed [3]. And, noise-shaping is realized by saving the residue voltage at the end of 9-bit SAR-ADC on an integrator and putting the voltage into the next SAR transition procedure through multiple input comparator. The residue voltage can be expressed as

$$V_{\text{res,SAR}} = V_{\text{in}} - \sum_{k=1}^{N-1} (-1)^{D_{\text{out}}(k)+1} \times \frac{V_{\text{ref}}}{2^{N-k}} \tag{1}$$

Where V_{in} is the input voltage, V_{ref} is the high reference voltage, N is the number of SAR transition steps, and D_{out} is the digital output code. Unfortunately, the residue voltage generated by the final comparison, as given in Eq. 1, is not able to apply to the passive integrator directly [5]. It should be plus or minus one LSB after the comparison is finished. In this design, one LSB means $V_{\text{ref}}/2^N$. In order to get a proper noise-shaping property with 9-bit SAR ADC, the error feedback voltage should be

$$\begin{aligned} V_{\text{res,NS}} &= V_{\text{in}} - \sum_{k=0}^{N-1} (-1)^{D_{\text{out}}(k)+1} \times \frac{V_{\text{ref}}}{2^{N-k}} \\ &= V_{\text{res,SAR}} - (-1)^{D_{\text{out}}(0)+1} \times \frac{V_{\text{ref}}}{2^N} \\ &= V_{\text{res,SAR}} - (-1)^{D_{\text{out}}(0)+1} \times \frac{C_{\text{LSB}}}{C_t} \times \frac{V_{\text{ref}}}{4} \end{aligned} \tag{2}$$

where C_{LSB} is the capacitance of the least significant bit, C_t is the total capacitance connecting with the sampling switch.

We summarize the SAR logic with the switching method in Algorithm 1. With the switching procedure complete, the voltage on the top plate of DAC array can be expressed as

$$\begin{aligned} V_{\text{t,p}} &= V_{\text{ip}} + (-D_{\text{out}}(N-1)+1)\frac{V_{\text{ref}}}{2} - D_{\text{out}}(N-2)\frac{V_{\text{ref}}}{4} \\ &\quad + \sum_{k=1}^{N-3} (-D_{\text{out}}(k)+1)\frac{V_{\text{ref}}}{2^{N-k}} \\ &= \frac{1}{2}V_{\text{res,SAR}} + \frac{V_{\text{ref}}}{2} + \sum_{k=1}^{N-3}\frac{V_{\text{ref}}}{2^{N-k}} \\ &= \frac{1}{2}V_{\text{res,SAR}} + \frac{3V_{\text{ref}}}{4} - \frac{V_{\text{ref}}}{2^{N-1}} \approx \frac{3}{4}V_{\text{ref}} \end{aligned} \tag{3}$$

From Eq. 2, the residual voltage generated by SAR transition should be plus or minus $V_{ref}/4 \times 1/2^7$. Thus, we proposed a new method to achieve the error feedback voltage, as shown in Fig. 1 and Fig. 2. After the last comparison step at each converter period, we share the charge from a capacitor (C_{00}) charged to V_{ref} to the input of the comparator. If the capacitance of C_{00} is the same as C_0, the voltage after charge sharing is given by

$$V_{\text{t,p}} = \frac{3/4V_{\text{ref}}2^{N-2}C_0 + V_{\text{ref}}C_0}{(2^{N-2}+1)C_0} \approx \frac{3}{4}V_{\text{ref}} + \frac{1}{2^N}V_{\text{ref}} \tag{4}$$

Therefore, the error feedback voltage is achieved by adding a simple circuit from a typical SAR ADC. We apply the charged capacitor to the negative DAC array if $D_{\text{out}}(0) = 1$ and vice versa.

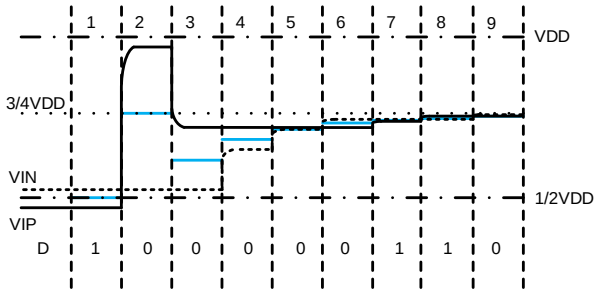

Fig. 3. Waveform of DAC switching procedure

Algorithm 1 OSSI and HBSI method

Input: input parameters V_{in}, V_{ip}
Output: output Dout[8:0], $V_{\text{res,NS}}$

Initial: $V_{\text{cap,N,i}} \leftarrow 0$, $V_{\text{cap,P,i}} \leftarrow 0$, $D_{\text{out}}[8:0] \leftarrow 0$, $V_{\text{cap,P,00}} \leftarrow V_{\text{cm}}$
$V_{\text{cap,N,MSB}} \leftarrow V_{\text{cm}}$, $V_{\text{cap,P,MSB}} \leftarrow V_{\text{cm}}$, $V_{\text{cap,P,00}} \leftarrow V_{\text{cm}}$
MSB: set $k \leftarrow 8$
if $V_{ip} \geq V_{in}$ **then**
  Dout[MSB] $\leftarrow 1$
  $V_{\text{cap,N,MSB}} \leftarrow V_{\text{ref}}$, $V_{\text{cap,N,i}} \leftarrow V_{\text{cm}}$ $\quad i = 0 : \text{MSB} - 1$, $V_{\text{cap,N,00}} \leftarrow V_{\text{ref}}$
else
  $V_{\text{cap,P,MSB}} \leftarrow V_{\text{ref}}$, $V_{\text{cap,P,i}} \leftarrow V_{\text{cm}}$ $\quad i = 0 : \text{MSB} - 1$, $V_{\text{cap,P,00}} \leftarrow V_{\text{ref}}$
end if
$k \leftarrow k - 1$
if Dout[MSB] $= 1$ **then**
  if $V_{ip} \geq V_{in}$ **then**
    Dout[k] $\leftarrow 1$,$V_{\text{cap,P,MSB}} \leftarrow 0$
  else
    $V_{\text{cap,N,MSB}} \leftarrow V_{\text{cm}}$
  end if
else
  if $V_{ip} \geq V_{in}$ **then**
    Dout[k] $\leftarrow 1$, $V_{\text{cap,P,MSB}} \leftarrow V_{\text{cm}}$
  else
    $V_{\text{cap,N,MSB}} \leftarrow 0$
  end if
end if
$k \leftarrow k - 1$
while $k \geq 1$ **do**
  if Dout[MSB] $= 1$ **then**
    if $V_{ip} \geq V_{in}$ **then**
      Dout[k] $\leftarrow 1$, $V_{\text{cap,N,k+1}} \leftarrow V_{\text{ref}}$
    else
      $V_{\text{cap,P,k+1}} \leftarrow V_{\text{cm}}$
    end if
  else
    if $V_{ip} \geq V_{in}$ **then**
      Dout[k] $\leftarrow 1$, $V_{\text{cap,N,k+1}} \leftarrow V_{\text{cm}}$
    else
      $V_{\text{cap,P,k+1}} \leftarrow V_{\text{ref}}$
    end if
  end if
  $k \leftarrow k - 1$
end while
LSB:
if $V_{ip} \geq V_{in}$ **then**
  Dout[0] $\leftarrow 1$
end if

1-st order passive filter and dynamic DC offset design: The noise-shaping property needs a filter to realize it. We apply a 1-st order passive filter in the proposed circuits. As Fig. 1 shows, we sample the residue voltage from the DAC capacitance array on sampling capacitor C_{ns}, and then share the charge with C_{int} which acts as an integrator. The transfer function of the passive filter can be described as

$$H(z) = \frac{(1-\alpha)\beta}{1-(1-\beta)z^{-1}} \tag{5}$$

Where α is $C_{\text{ns}}/(C_t + C_{\text{ns}})$, β is $C_{\text{ns}}/(C_{\text{int}} + C_{\text{ns}})$.

In order to set a proper DC voltage of the passive filter. The sampling capacitor (C_{ns}) is separated into two parts: $C_{\text{ns,p1}}$,$C_{\text{ns,p2}}$. And $C_{\text{ns,p1}}$,$C_{\text{ns,p2}}$ are set to GND and V_{ref} respectively in the reset phase. In the sampling phase, they are connected and utilized to sample the voltage on the DAC capacitance array. Then, C_{int} could share the charge from the sampling capacitor in the integration phase. The DC voltage in the passive filter could be set to $3/4V_{\text{ref}}$ if $C_{\text{ns,p1}}$ is equal to $C_{\text{ns,p2}}$. It is the same as the DC voltage shown by Eq. 3.

Using the top plate sampling, the common mode voltage at the compactor varies with the time at which each bit is generated, as is shown in Fig.3. However, the voltage (V_{int}) on the integrator capacitor will keep constant if we are not going to do anything. It would lead to a wrong path gain g. As a result, the noise-shaping loop does not work or is unstable. At the first conversion, the common-mode voltage is $1/2$ VDD. After the first decision has been made, the voltage on the VIP net would be changed to $V_{ip,1} + 1/2$VDD, and the voltage on the VIP net keep the same ($V_{in,2} = V_{in,1}$). Thus, the common-mode voltage at the second conversion is $3/4$ VDD. Then, the voltage on the VIN net would drops to $V_{in,3} = V_{in,2} - 1/4$VDD after the second conversion. Therefore, the common-mode voltage is $5/8$ VDD, and so on. The common-mode voltage at the k-conversion is given by

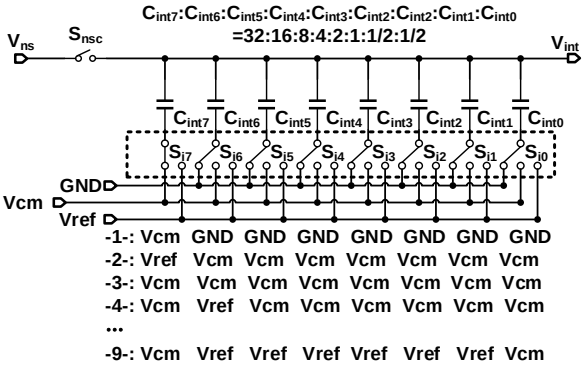

Fig. 4. Passive integrator with energy-efficient switching method

$$V_{CM,k} = \begin{cases} 1/2V_{ref}, & k = 1 \\ 3/4V_{ref}, & k = 2 \\ \left(\frac{3}{4} - \frac{1}{2^k}\right)V_{ref}, & k \geq 3 \end{cases} \tag{6}$$

To realize a proper noise-shaping property, V_{int} should have the same common mode voltage as the top plate of the capacitor array. Thus the path gain would remain unchanged at each converter step. In our design, the integrator capacitor is split into many parts: $C_{\text{int,p1}}, C_{\text{int}} < 7:0 >$. And, the equation ($C_{\text{int,p1}} = \sum C_{\text{int}} < i >$) is satisfied. Similarly, the energy-efficient switching method also can be utilized for switching integrator capacitance array.

The switching procedure can be shown in Fig. 4, and DC voltage of the passive integrator is marked in Fig. 3. During each conversion step, we dynamic adjust it's DC offset voltage by connecting the integrator capacitor array to V_{cm}, V_{ref} or GND. Therefore, a correct and fixed path gain would be achieved.

Switching energy and performance analysis: We can divide the total energy consumption in noise-shaping SAR ADC into five main parts: DAC, logic, sampling switch, comparator, and integrator. In the passive noise-shaping SAR ADC, the switching energy on the integrator capacitance is the main part of the energy consumption of the integrator. From the calculation method in Ref [6], the switching energy is given by

$$E_{\text{sw,int}} = C_0 V_{\text{ref}}^2 \times \left(6 + \frac{5}{2} + \frac{9}{8} + \frac{17}{32} + \frac{33}{128} + \frac{65}{512}\right) \tag{7}$$

And, the reset energy is $15.75C_0V_{\text{ref}}^2$. From Ref [3],the switching energy of DAC capacitor in a 9-bit SAR ADC is 8 CV_{ref}^2, and the reset energy is 15.6 CV_{ref}^2. Therefore, the total switching energy and reset energy are respectively 29 CV_{ref}^2 and 47.1 CV_{ref}^2.

In this noise shaping loop, C_{ns} is 32C, C_t is 128C, and C_{int} is 128C. Therefore, the total capacitance is 576C. The noise transfer function (NTF) is $1 - 0.8z^{-1}$. If the oversampling ratio (OSR) is 8, the signal-to-quantization-noise ratio (SQNR) can be improved by 18.8dB (3bit). As a result, we can achieve a 12-bit oversampling SAR ADC with the noise-shaping method. However, a 12-bit oversampling SAR ADC could be realized by a 10-bit Nyquist SAR ADC at an OSR of 16 without a noise-shaping method. In addition, a 10-bit Nyquist SAR ADC has a total capacitance of 512C with the same energy-efficient switching method.

As shown in Table 1, we compare several 12-bit oversampling SAR ADC types. If the input capacitance is the same, the oversampling SAR ADC without noise-shaping would need more energy to realize a 12-bit SAR ADC, as a large OSR is required. To show the advantage of the proposed noise-shaping SAR ADC, we keep the energy consumption and the total capacitance approximately is same. A smaller input capacitance and lower OSR is required than others in Table 1 to realize a 12-bit SAR ADC.

Table 1: Comparison of switching method for 12-bit oversampling SAR ADC

Switching scheme	S&H [7]	Tri-level [8]	VMS [1]	OSSI [3]	COSS [9]	Proposed
$E_{avg,sw}$ (CV_{ref}^2)	255.5	42.41	31.9	15.8	26.54	30
$E_{avg,rst}$ (CV_{ref}^2)	0	0	0	31.2	0	47
Total cap.	512	512	512	512	512	576
Input cap.	256	256	256	256	256	128
OSR	16	16	16	16	16	8
E_{tot} (CV_{ref}^2)	4088	678.56	510.4	752	424.64	608

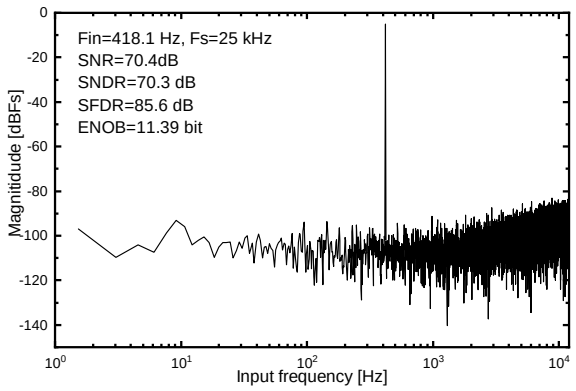

Fig. 5. Simulated PSD with -0.68 dBFS input signal

Simulation and analysis: We construct the novel noise-shaping SAR ADC in TSMC 180nm 1P4M CMOS technology. Fig. 5 shows the simulation result in TT corner at 27 degrees with transient noise enable. The slope of the first-order noise-shaping of $(1 - 0.8z^{-1})$ is clearly seen from Fig. 5. The effective number of bits (ENOB) is improved to 11.39 when OSR is 8. However, the basic architecture is a 9-bit SAR ADC with an efficient switching method. Thanks to the noise shaping loop in the SAR ADC, we get 2∼3 bit improvement, which is more than 1.5-bit without a noise-shaping effect when OSR is 8. On the other hand, the total power consumption is 130nW, as shown in Fig. 5. The noise-shaping loop cost of about 44nW from the simulation result. It costs more energy than DAC capacitance, which accords with the theory analysis.

Table 2 shows the comparison of the performance of the proposed noise-shaping SAR ADC with prior SAR-ADC. It can achieve 70dB SNDR and 171dB Schreier FoM, which is in-line with state-of-the-art. Compared with prior SAR-ADCs, its input capacitor is smaller than others, which means that the input signal requires driving a smaller capacitor load. It is a benefit to decreasing the power consumption of the input buffer.

Table 2: Performance summary and comparison

Reference	TCASI-16 [9]	TCASI-15 [3]	JSSC-19 [4]	Proposed
Noise shaping	no	no	2nd-order	1st-order
Technology	180nm	180nm	40nm	180nm
Supply voltage(V)	1.8	0.6	1.1	0.6
input cap.(C)	512	256	512	128
Sampling(kHz)	10000	20	8400	25
Power(nW)	820000	38	143000	130
OSR	1	1	16	8
SNDR(dB)	66.9	58.3	78.4	70.3
ENOB(bit)	10.8	9.4	12.7	11.4
FOMs(dB)	165	173	171	171

$$\text{FOMs} = \text{SNDR} + 10\log(\frac{Fs/(2\text{OSR})}{\text{Power}})$$

Conclusion: A passive first-order noise-shaping SAR ADC with an energy-efficient switching method is presented. In the proposed scheme, we use the same switching step to adjust the DC voltage on the integrator capacitor to realize the noise shaping effect. Furthermore, utilizing the property of the switching method, which leads to the final voltage on the DAC capacitor would be 3/4 V_{DD}, we add a simple circuit to get the error feedback voltage. In addition, the novel architecture has been verified in TSMC 180nm CMOS technology from simulation. The result showed a

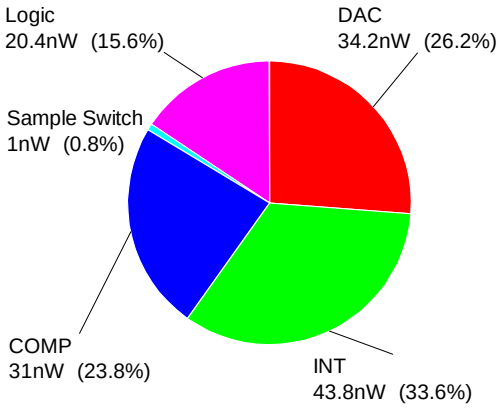

Fig. 6. Simulated power consumption of each part

171dB Schreier FoM and 11.4 ENOB with a 0.6V supply voltage and 25kHz sampling rate.

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