Posted on Authorea 5 Jul 2022 — The copyright holder is the author/funder. All rights reserved. No reuse without permission. — https://doi.org/10.22541/au.165703709.98852173/v1 — This a preprint and has not been peer reviewed. Data may be preliminary.

A 16.7-Gb/s full-transition avoidance PAM-4 2-tap FFE transmitter with shunt switches for display interfaces

Jiyun Han[1], Eunji Song[1], Hyeongmin Seo[1], Hyunwoo Im[1], and Jaeduk Han[1]

[1]Hanyang University

July 5, 2022

Abstract

This paper describes a channel-loss-tolerant 16.7-Gb/s PAM-4 transmitter with feed-forward equalization (FFE) for display interfaces. The proposed transmitter adopts full transition avoidance (FTA) coding in combination with the 2-tap FFE to enhance the worst-case horizontal eye-opening in the presence of inter-symbol interference (ISI) and shunt switches to reduce power consumption. The transmitter test chip was fabricated in a 28-nm CMOS process and occupied 0.04 mm2. The design achieved 16.7-Gb/s (corresponding to 10 Gbaud/s) with a 0.20x wider horizontal eye-opening for a >7.2 dB loss channel while consuming 107.6mW (corresponding to 6.4 pJ/bit) from the 1.2-V supply.

A 16.7-Gb/s full-transition avoidance PAM-4 2-tap FFE transmitter with shunt switches for display interfaces

Jiyun Han, Eunji Song, Hyeongmin Seo, Hyunwoo Im and Jaeduk Han

This paper describes a channel-loss-tolerant 16.7-Gb/s PAM-4 transmitter with feed-forward equalization (FFE) for display interfaces. The proposed transmitter adopts full transition avoidance (FTA) coding in combination with the 2-tap FFE to enhance the worst-case horizontal eye-opening in the presence of inter-symbol interference (ISI) and shunt switches to reduce power consumption. The transmitter test chip was fabricated in a 28-nm CMOS process and occupied 0.04 mm2. The design achieved 16.7-Gb/s (corresponding to 10 Gbaud/s) with a 0.20x wider horizontal eye-opening for a >7.2 dB loss channel while consuming 107.6mW (corresponding to 6.4 pJ/bit) from the 1.2-V supply.

Introduction: As high-resolution display systems require the massive transmission of graphic data, data rates of high-speed interfaces for display SoCs continue to grow. For example, intra-panel interfaces to support 5-10 Gb/s per-lane data rates for 8K displays and 15+Gb/s for next-generation ones [1–3]. However, the channel bandwidths of such display systems are severely limited due to loss and reflections from long PCB traces and FPC (Flexible Printed Circuit) structures. Therefore, transceivers for the display interfaces should adopt advanced signaling (such as PAM-4 [4–7]) and equalization (such as FFE [8, 9]) techniques to achieve such high data rates in energy-efficient ways. However, the voltage mode FFE driver suffers from high power consumption, and the PAM-4 signaling yields high sensitivity to residual ISIs. Therefore, typical PAM-4 transceivers require additional forwarded error correction (FEC) schemes to achieve a low bit-error ratio (BER), which are not feasible for display interfaces, as the receivers are implemented in legacy technologies. In display interfaces, the source driver is fabricated in long-length and high-voltage processes to drive the display panel. Therefore, additional low-overhead signaling and/or coding schemes are required for the display interfaces to enable the PAM-4 signal transmission without relying on digital-intensive FECs.

In this paper, we introduce a voltage-mode PAM-4 FFE transmitter with shunt switches for high-speed display interfaces. The voltage-mode output driver in the proposed transmitter generates PAM-4 FFE signals by controlling shunt switches (which are originally used for NRZ FFE operation in [10]) to save the

Posted on Authorea 5 Jul 2022 — The copyright holder is the author/funder. All rights reserved. No reuse without permission. — https://doi.org/10.22541/au.165703709.98852173/v1 — This a preprint and has not been peer reviewed. Data may be preliminary.

final output driver power consumption. In addition to that, we propose the full-transition avoidance (FTA) encoding scheme to further enhance the signal integrity by limiting transitions that produce significant inter-symbol interferences (ISI).

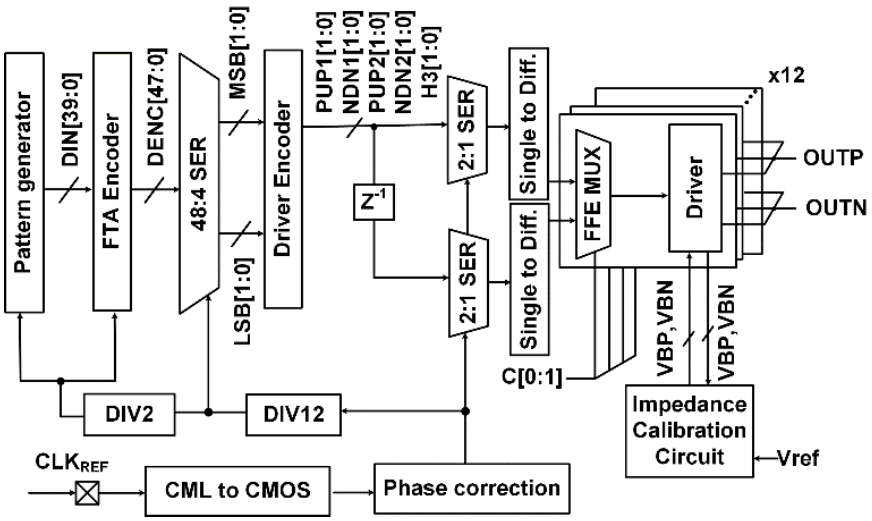


Fig. 1 *Block diagram of the proposed PAM-4 transmitter.*

PAM-4 transmitter with FTA and shunt switches: Fig. 1 shows the structure of the 16.7-Gb/s transmitter that implements the 2-tap PAM-4 FFE operation with real-time FTA encoding. The 40-bit raw input data stream (DIN[39:0]) is manipulated by the following FTA encoder of which output signals (DENC[47:0]) are provided to the 48-to-4 serializer, which generates the most significant bits (MSB[1:0]) and least significant bits (LSB[1:0]) for the subsequent frontend circuits. The output drivers are sliced to support the 2-tap PAM-4 FFE operation with its 2-bit control signal (C[1:0]) to set the strength of main and post taps.

Posted on Authorea 5 Jul 2022 — The copyright holder is the author/funder. All rights reserved. No reuse without permission. — https://doi.org/10.22541/au.165703709.98852173/v1 — This a preprint and has not been peer reviewed. Data may be preliminary.

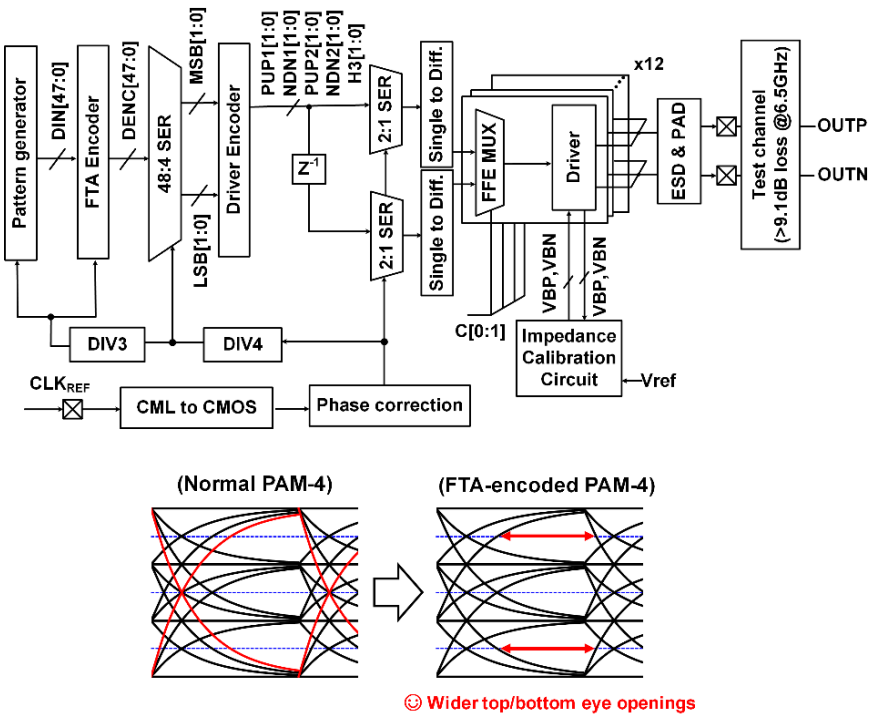


Fig. 2 *Conceptual eye diagram of FTA encoding.*

Posted on Authorea 5 Jul 2022 — The copyright holder is the author/funder. All rights reserved. No reuse without permission. — https://doi.org/10.22541/au.165703709.98852173/v1 — This a preprint and has not been peer reviewed. Data may be preliminary.

Input data (5B)					Mapping group 1 (3Q starting with -3)			Mapping group 2 (3Q starting with +3)		
D[0]	D[1]	D[2]	D[3]	D[4]	C[0]	C[1]	C[2]	C[0]	C[1]	C[2]
0	0	0	0	0	-3	-3	-3	3	3	3
0	0	0	0	1	-3	-3	-1	3	3	1
0	0	0	1	0	-3	-3	1	3	3	-1
0	0	0	1	1	-3	-1	-3	3	1	3
0	0	1	0	0	-1	-3	-3	-1	-3	-3
0	0	1	0	1	-1	-3	-1	-1	-3	-1
0	0	1	1	0	-1	-3	1	-1	-3	1
0	0	1	1	1	-1	-1	-3	-1	-1	-3
0	1	0	0	0	-1	-1	-1	-1	-1	-1
0	1	0	0	1	-1	-1	1	-1	-1	1
0	1	0	1	0	-1	-1	3	-1	-1	3
0	1	0	1	1	-1	1	-3	-1	1	-3
0	1	1	0	0	-1	1	-1	-1	1	-1
0	1	1	0	1	-1	1	1	-1	1	1
0	1	1	1	0	-1	1	3	-1	1	3
0	1	1	1	1	-1	3	-1	-1	3	-1
1	0	0	0	0	-1	3	1	-1	3	1
1	0	0	0	1	-1	3	3	-1	3	3
1	0	0	1	0	1	-3	-3	1	-3	-3
1	0	0	1	1	1	-3	-1	1	-3	-1
1	0	1	0	0	1	-3	1	1	-3	1
1	0	1	0	1	1	-1	-3	1	-1	-3
1	0	1	1	0	1	-1	-1	1	-1	-1
1	0	1	1	1	1	-1	1	1	-1	1
1	1	0	0	0	1	-1	3	1	-1	3
1	1	0	0	1	1	1	-3	1	1	-3
1	1	0	1	0	1	1	-1	1	1	-1
1	1	0	1	1	1	1	1	1	1	1
1	1	1	0	0	1	1	3	1	1	3
1	1	1	0	1	1	3	-1	1	3	-1
1	1	1	1	0	1	3	1	1	3	1
1	1	1	1	1	1	3	3	1	3	3

Fig. 3 *Conceptual eye diagram of FTA encoding.*

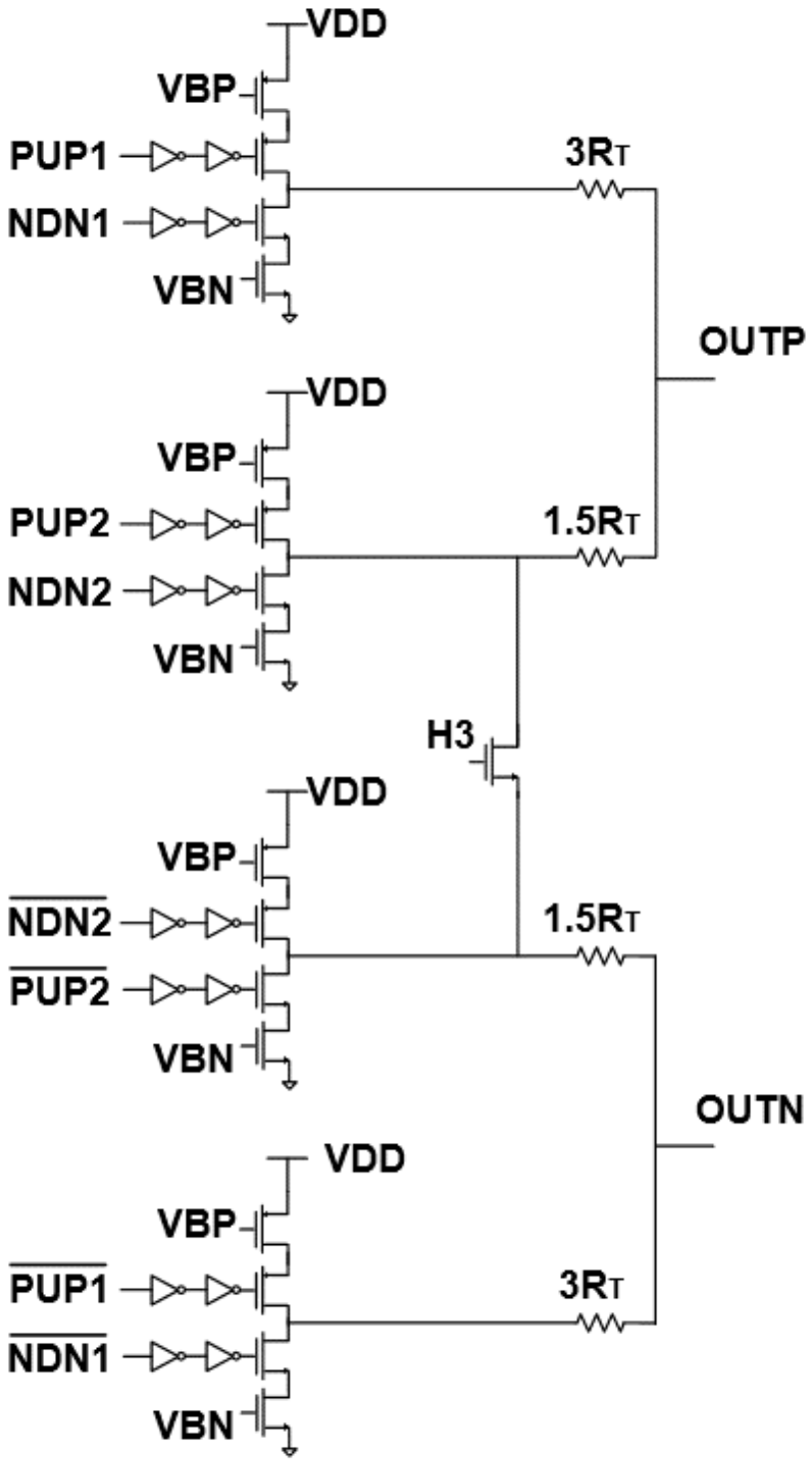
FTA encoding: While the PAM-4 signaling and FFE equalization techniques remove ISI significantly, further signal quality improvements in transmit side are preferred to relax the equalization requirements on receive side, especially for display intra-panel links as their receive display driver ICs (DDIs) are fabricated in legacy technologies and are incapable of high-performance equalization and/or FEC operations. In particular, large-signal transitions between 00 and 11 symbols in PAM-4 waveforms need to be addressed, as they degrade the top and bottom eye openings significantly. The proposed FTA encoding scheme is therefore introduced to expand the eye openings by avoiding the full-scale data transitions between the lowest (00) and highest (11) voltage levels among the four possible PAM-4 voltage levels. Fig. 2 shows a conceptual eye diagram of the FTA-encoded PAM-4 signal in comparison with a conventional PAM-4 eye diagram. In the conventional PAM-4 eye diagram, owing to the data transitions between the highest and lowest voltage levels, the top and bottom eye widths are reduced more than the middle eye width. The FTA encoding removes the abrupt transitions and enhances the worst-case eye openings, as shown in the figure.

For the effective hardware implementation of the FTA scheme with minimal power and latency overheads, we propose a 5-binary-to-3-quaternary (5B3Q) encoding technique with its embodiment summarized in Fig. 3. Each of the mapping groups 1 and 2 excludes 3Q sequences starting with a specific quaternary code; for

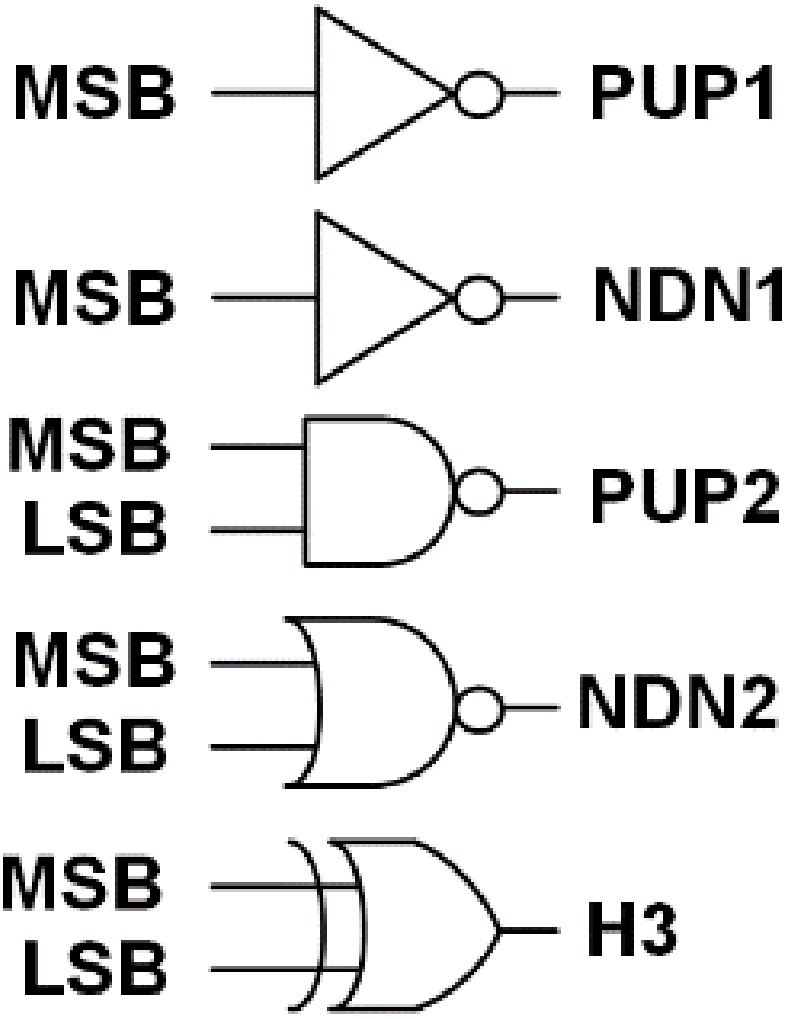
example, mapping group 1 does not include 3Q sequences starting with +3, whereas mapping group 2 does not include 3Q sequences starting with -3. For instance, 3Q (-3, x, y) is included in mapping group 1, and (+3, x, y) is included in mapping group 2. The FTA encoder generates a 3Q code for its 5-bit binary input sequence based on its corresponding mapping entry in the figure and the value of the previous 3Q code. To be specific, when the previous 3Q code ends with -3, the FTA encoder selects a 3Q code from mapping group 1. On the other hand, when the previous 3Q code ends with +3, the FTA encoder selects its output from mapping group 2. If the previous 3Q code neither ends with -3 nor +3, the FTA encoder arbitrary selects either from group 1 or 2, depending on the convenience of digital synthesis. In this way, the data transitions between the top and bottom ends are avoided, which expands the top and bottom eye widths of the PAM-4 eye diagram significantly. As the look-up table entry only contains 32 entries per output, the 5B3Q encoders are implemented simply by synthesizing the look-up table directly.

Posted on Authorea 5 Jul 2022 — The copyright holder is the author/funder. All rights reserved. No reuse without permission. — https://doi.org/10.22541/au.165703709.98852173/v1 — This a preprint and has not been peer reviewed. Data may be preliminary.

Posted on Authorea 5 Jul 2022 — The copyright holder is the author/funder. All rights reserved. No reuse without permission. — https://doi.org/10.22541/au.165703709.98852173/v1 — This a preprint and has not been peer reviewed. Data may be preliminary.



Posted on Authorea 5 Jul 2022 — The copyright holder is the author/funder. All rights reserved. No reuse without permission. — https://doi.org/10.22541/au.165703709.98852173/v1 — This a preprint and has not been peer reviewed. Data may be preliminary.



(a) (b)

Fig. 4 *(a) Schematic of proposed voltage mode driver slice with a shunt switch, and (b) schematic of driver encoder.*

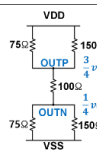
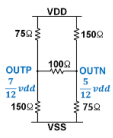
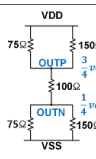
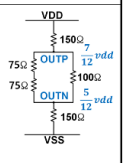
Type	Conventional SST driver		Proposed SST driver with shunt mode enabled	
Input (MSB, LSB)	(1,1) or (0,0)	(1,0) or (0,1)	(1,1) or (0,0)	(1,0) or (0,1)
Equivalent circuit				
Power consumption	$P_{sig_A} = \frac{vdd^2}{4R}$	$P_{sig_B} = \frac{17vdd^2}{36R}$	$P_{sig_A} = \frac{vdd^2}{4R}$	$P_{sig_B} = \frac{5dd^2}{36R}$
Total power consumption	$P_{total} = \frac{1}{2}\left(\frac{vdd^2}{4R} + \frac{17vdd^2}{36R}\right) = \frac{13vdd^2}{36R}$		$P_{total} = \frac{1}{2}\left(\frac{vdd^2}{4R} + \frac{5vdd^2}{36R}\right) = \frac{7vdd^2}{36R}$	

Fig. 5 *Comparison of PAM-4 driver schemes.*

Posted on Authorea 5 Jul 2022 — The copyright holder is the author/funder. All rights reserved. No reuse without permission. — https://doi.org/10.22541/au.165703709.98852173/v1 — This a preprint and has not been peer reviewed. Data may be preliminary.

Voltage mode driver with shunt switch: Fig. 4(a) shows the structure of the proposed output driver slice with a shunt switch. Compared with previous PAM-4 transmitters [6, 7], the design avoids the use of current-mode branches to fully take advantage of voltage-mode drivers in terms of energy efficiency. The driver is divided into 12 slices, and each slice is composed of four impedance-controlled pull-up/down switches and one shunt switch. The switches are configured by their control signals (PUP1, NDN1, PUP2, and NDN2 for the pull-up/down switches, and H3 for the shunt switch) fed from the driver encoder, of which schematic is briefly illustrated in Fig. 4(b). Fig. 5 presents a comparative summary of the driver operation, including equivalent circuit diagrams with comparisons with conventional voltage drivers. It should be noted that the total power consumption of the PAM-4 drivers should be the average of the value of power consumption when its input symbols are either identical (00 or 11) or different (01 or 10) if the four symbol levels appear with uniform probabilities. For conventional voltage-mode PAM-4 drivers, the average signaling power consumption is determined by the following expressions:

$$P_{\text{total}} = \frac{13\text{vdd}^2}{36R} \quad (1)$$

Meanwhile, the average signaling power consumption of the proposed output driver is determined as follows:

$$P_{\text{total}} = \frac{7\text{vdd}^2}{36R} \quad (2)$$

These observations reveal that the use of shunt switch reduces the power consumption significantly, by a factor of 3/7 [?] 43%.

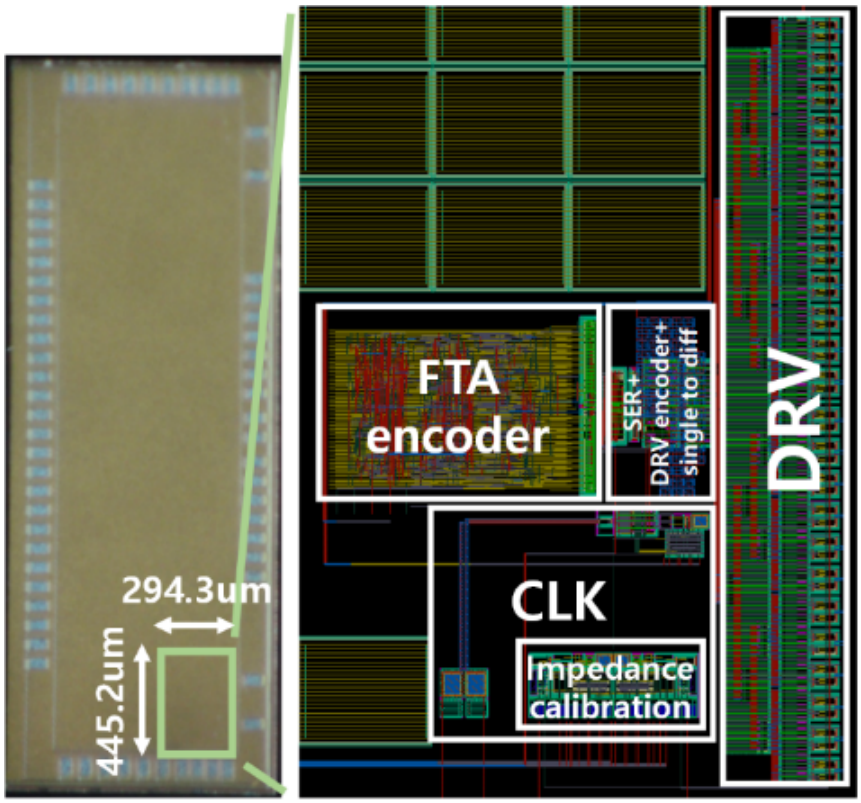
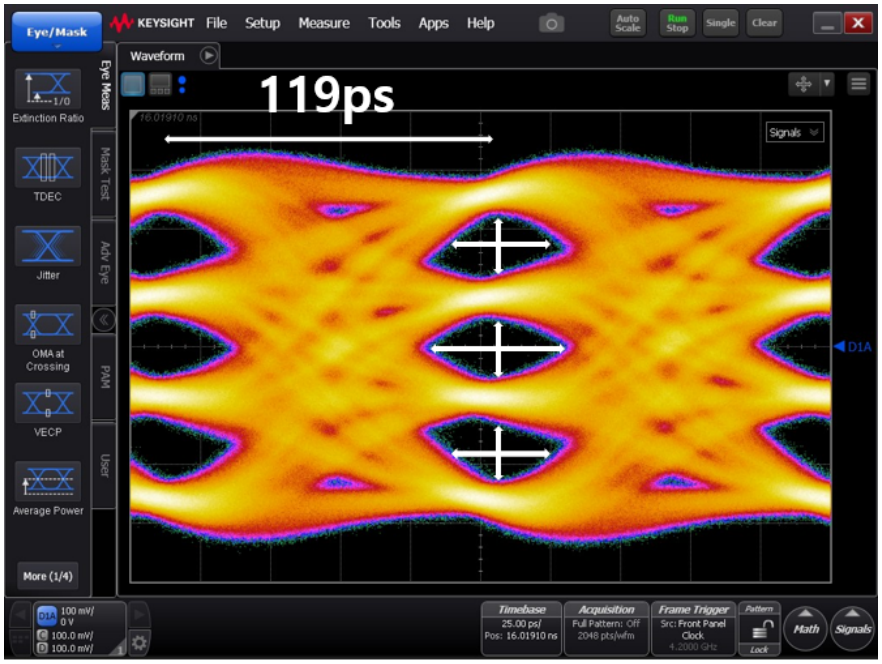


Fig. 6 *Chip micrograph and layout.*

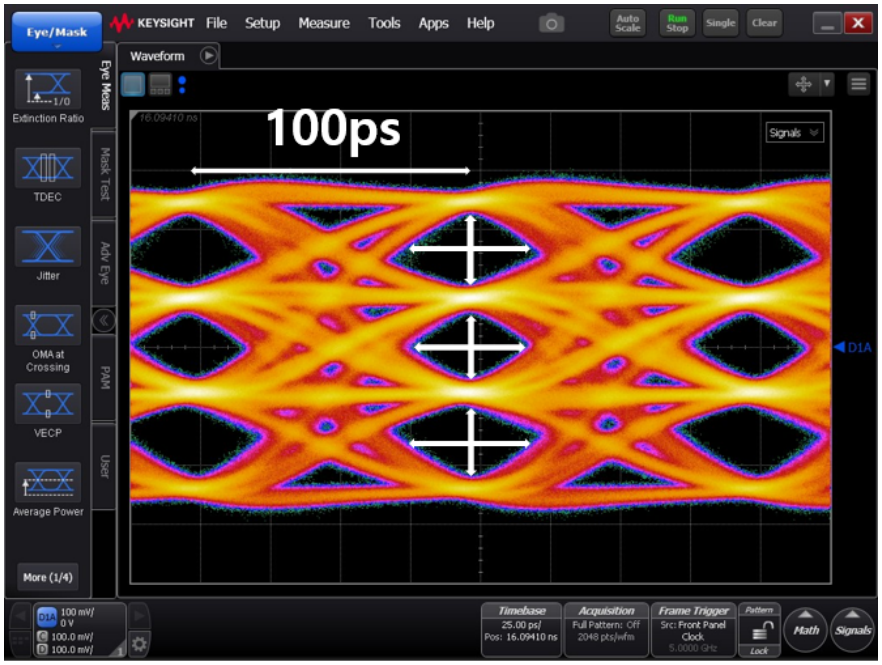
Measurement results: In order to demonstrate the PAM-4 FFE and FTA-encoding operation, a prototype PAM-4 transmitter is implemented in a 28-nm CMOS technology and its chip micrograph is shown in Fig.

Posted on Authorea 5 Jul 2022 — The copyright holder is the author/funder. All rights reserved. No reuse without permission. — https://doi.org/10.22541/au.165703709.98852173/v1 — This a preprint and has not been peer reviewed. Data may be preliminary.

6. The fabricated transmitter design occupies a compact die area of 0.04 mm2. Fig. 7 shows the measured eye diagrams at 16.7-Gb/s without the FTA encoding (corresponding to 8.4 Gbaud/s) and with the FTA encoding (corresponding to 10 Gbaud/s) respectively applied to a PRBS31 test pattern. The eye diagrams are measured at 1.2-V supply, by probing the output of a differential test channel composed of a pair of bonding wires, 3-cm PCB traces, 2.9-mm connectors, and an additional 7.2-dB loss differential trace structure at 5GHz. As shown in the eye diagrams, the top/bottom openings are enhanced significantly by the application of the proposed FTA encoding. For numerical comparisons, the eye width and height openings of the top, middle, and bottom of the PAM-4 eye diagrams are measured by the oscilloscope and annotated in Fig. 7. The horizontal widths of the top and bottom eyes are widened by 20.2% and 20.7% when the FTA encoding is applied. The transmitter consumed 107.6mW, and the power breakdown is presented in Fig. 8. The excessive power consumption is mainly contributed to the oversizing of pre-drivers in the prototype design, which could be reduced significantly after further optimizations. The performance of the proposed PAM-4 transmitter is summarized and compared with previous NRZ/PAM-4 transmitter designs that achieved 16-32 Gb/s/lane data rates in Fig. 9. Thanks to the ISI-tolerant FTA coding scheme, the presented design achieved a 15+Gb/s data rate with sufficiently improved horizontal/vertical eye openings, which removes the need for additional error correction schemes for asymmetric transceivers for next-generation display interfaces.



Without FTA encoding (8.4 Gbaud/s)			
Eye width(-ps)		Eye height(-mV)	
Top	34.95	Top	96.0
Middle	47.04	Middle	96.0
Bottom	34.95	Bottom	96.0



With FTA encoding (10 Gbaud/s)			
Eye width(-ps)		Eye height(-mV)	
Top	42.02	Top	121.3
Middle	38.44	Middle	109.33
Bottom	42.20	Bottom	116.0

Fig. 7 *Measured transmitter output eye diagrams at 16.7Gb/s without and with FTA encoding.*

Posted on Authorea 5 Jul 2022 — The copyright holder is the author/funder. All rights reserved. No reuse without permission. — https://doi.org/10.22541/au.165703709.98852173/v1 — This a preprint and has not been peer reviewed. Data may be preliminary.

Posted on Authorea 5 Jul 2022 — The copyright holder is the author/funder. All rights reserved. No reuse without permission. — https://doi.org/10.22541/au.165703709.98852173/v1 — This a preprint and has not been peer reviewed. Data may be preliminary.

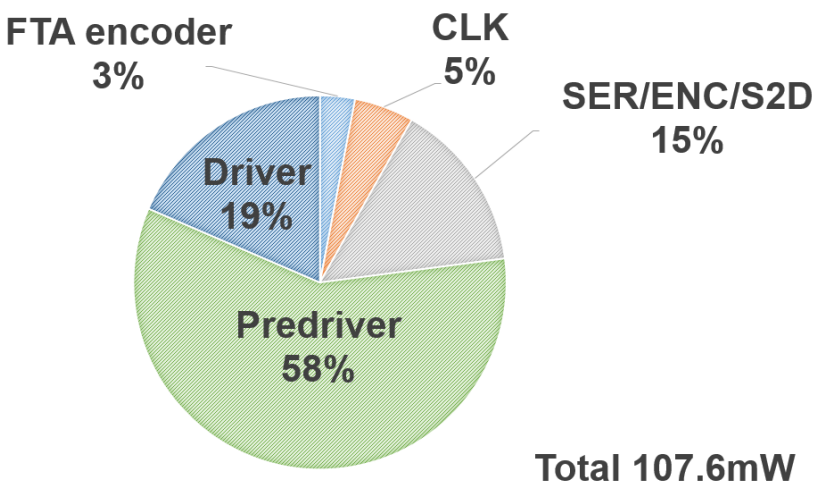


Fig. 8 *Power breakdown of proposed transmitter.*

Conclusion: This paper describes design techniques for a PAM-4 transmitter with enhanced top and bottom eye openings. The transmitter incorporates a 2-tap FFE driver, serializers, clocking circuits, and an impedance calibration circuit. An energy-efficient PAM-4 driver is realized by introducing shunt switches. The FTA encoding scheme enhances the horizontal openings of the top and bottom eyes by 20.2% and 20.7%, respectively, at 16.7-Gb/s.

Acknowledgments: Jiyun Han and Eunji Song contributed equally to this work. The research was sponsored in part by Samsung Research Funding & Incubation Center of Samsung Electronics under Project Number SRFC-IT2001-02 and the Institute of Information & Communications Technology Planning & Evaluation(IITP) grant funded by the Korea government(MSIT) (No.2020-0-01307).

Jiyun Han, Eunji Song, Hyeongmin Seo, Hyunwoo Im and Jaeduk Han (*Hanyang University, Seoul, Korea*)

E-mail: jdhan@hanyang.ac.kr

Posted on Authorea 5 Jul 2022 — The copyright holder is the author/funder. All rights reserved. No reuse without permission. — https://doi.org/10.22541/au.165703709.98852173/v1 — This a preprint and has not been peer reviewed. Data may be preliminary.

	This work	[4] TVLSI'21	[7] JSSC'17	[11] JSSC'08
Process [nm]	**28**	28	65	90
Supply voltage [V]	**1.2**	1.0	1.2	1.8
Data rate [Gb/s]	**16.7**	32	32	20
FFE taps	**2**	4	2	3
Architecture	**SST**	SST	SST	CML
Horizontal eye expansion	**O**	X	X	X
Channel loss [dB]	**>7.2**	N/A	13.5	N/A
Horizontal eye opening [UI]	**0.4**	0.16	0.06	N/A
Vertical eye opening [mV]	**109.33**	38	N/A	18
Test PRBS length	**31**	N/A	15	31
Power consumption [mW]	**107.6**	77.9	176.3	150
Energy efficiency [pJ/bit]	**6.4**	2.4	5.5	7.5
Active-area [mm^2]	**0.04**	0.56	0.074	0.19

Fig. 9 *Performance summary and comparisons with various 16-32Gb/s PAM-4 transmitters.*

References

1. Y. Lee et al., "12-Gb/s Over Four Balanced Lines Utilizing NRZ Braid Clock Signaling With No Data Overhead and Spread Transition Scheme for 8K UHD Intra-Panel Interfaces," *IEEE Journal of Solid-State Circuits* , 2019, **54** , 2, pp. 463-475, doi: 10.1109/JSSC.2018.2878814

2. J. Park, J. -H. Chae, Y. -U. Jeong, J. -W. Lee and S. Kim, "A 2.1-Gb/s 12-Channel Transmitter With Phase Emphasis Embedded Serializer for 55-in UHD Intra-Panel Interface," *IEEE Journal of Solid-State Circuits* , 2018, **53** , 10, pp. 2878-2888, doi: 10.1109/JSSC.2018.2859808

3. Y. -U. Jeong et al., "A 9Gb/s Wide Output Range Transmitter With 2D Binary-Segmented Driver and Dual-Loop Calibration for Intra-Panel Interfaces," *IEEE Transactions on Circuits and Systems II: Express Briefs* , 2020, **67** , 9, pp. 1589-1593, doi: 10.1109/TCSII.2020.3013420

4. F. Celik, A. Akkaya, A. Tajalli and Y. Leblebici, "A 32-Gb/s PAM-4 SST Transmitter With Four-Tap FFE Using High-Impedance Driver in 28-nm FDSOI," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* , 2021, **29** , 6, pp. 1132-1140, doi: 10.1109/TVLSI.2021.3068242

5. P. -J. Peng, Y. -T. Chen, S. -T. Lai and H. -E. Huang, "A 112-Gb/s PAM-4 Voltage-Mode Transmitter With Four-Tap Two-Step FFE and Automatic Phase Alignment Techniques in 40-nm CMOS," *IEEE Journal of Solid-State Circuits* , 2021, **56** , 7, pp. 2123-2131, doi: 10.1109/JSSC.2020.3038818

6. C. Fan, W. Yu, P. Mak and R. P. Martins, "A 40-Gb/s PAM-4 Transmitter Using a 0.16-pJ/bit SST-CML-Hybrid (SCH) Output Driver and a Hybrid-Path 3-Tap FFE Scheme in 28-nm CMOS," *IEEE Transactions on Circuits and Systems I: Regular Papers* , 2019, **66** , 12, pp. 4850-4861, doi: 10.1109/TCSI.2019.2936226

7. A. Roshan-Zamir, O. Elhadidy, H. Yang and S. Palermo, "A Reconfigurable 16/32 Gb/s Dual-Mode NRZ/PAM4 SerDes in 65-nm CMOS,"*IEEE Journal of Solid-State Circuits* , 2017, **52** , 9, pp. 2430-2447, doi: 10.1109/JSSC.2017.2705070

Posted on Authorea 5 Jul 2022 — The copyright holder is the author/funder. All rights reserved. No reuse without permission. — https://doi.org/10.22541/au.165703709.98852173/v1 — This a preprint and has not been peer reviewed. Data may be preliminary.

8. T. O. Dickson, H. A. Ainspan and M. Meghelli, "6.5 A 1.8pJ/b 56Gb/s PAM-4 transmitter with fractionally spaced FFE in 14nm CMOS," *IEEE International Solid-State Circuits Conference* , San Francisco, CA, USA, 2017, pp. 118-119, doi: 10.1109/ISSCC.2017.7870289

9. J. Han, Y. Lu, N. Sutardja, K. Jung and E. Alon, "Design Techniques for a 60 Gb/s 173 mW Wireline Receiver Frontend in 65 nm CMOS Technology," *IEEE Journal of Solid-State Circuits* , 2016,**51** , 4, pp. 871-880, doi: 10.1109/JSSC.2016.2519389

10. Y. Lu, K. Jung, Y. Hidaka and E. Alon, "Design and Analysis of Energy-Efficient Reconfigurable Pre-Emphasis Voltage-Mode Transmitters," *IEEE Journal of Solid-State Circuits* , 2013, **48** , 8, pp. 1898-1909, doi: 10.1109/JSSC.2013.2258790

11. J. Lee, M. -S. Chen and H. -D. Wang, "Design and Comparison of Three 20-Gb/s Backplane Transceivers for Duobinary, PAM4, and NRZ Data," *IEEE Journal of Solid-State Circuits* , 2008, **43** , 9, pp. 2120-2133, doi: 10.1109/JSSC.2008.2001934.

Hosted file

`figure_zip.pptx` available at https://authorea.com/users/493203/articles/575703-a-16-7-gb-s-full-transition-avoidance-pam-4-2-tap-ffe-transmitter-with-shunt-switches-for-display-interfaces