A 0.6V rail-to-rail regenerative comparator with a thyristor-based latch

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Abstract

A low voltage two-stage rail-to-rail regenerative comparator is presented. For the first time, a thyristor-based latch is introduced in this work, enabling the comparator's rail-to-rail operation. The proposed comparator is post-layout simulated in a standard 180nm CMOS technology. The results certify that the comparator's delay and power are less than 28ns and 230nW with 0.6V supply voltage and 1MHz sample rate. The total input-referred offset voltage (3std+mean) is less than 6.2mV over the entire rail-to-rail common-mode voltage range. In comparison with similar works the proposed comparator has the lowest delay and offset and achieves the best FOM.

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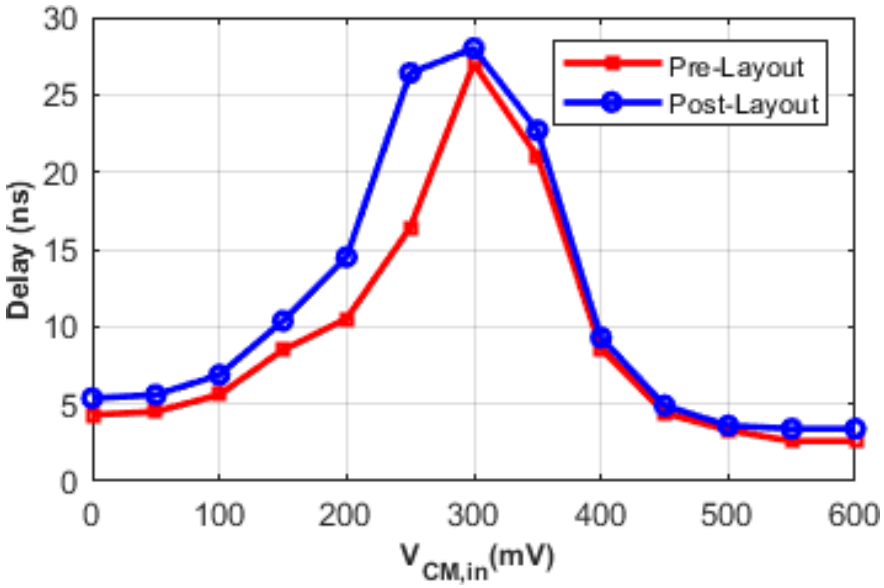
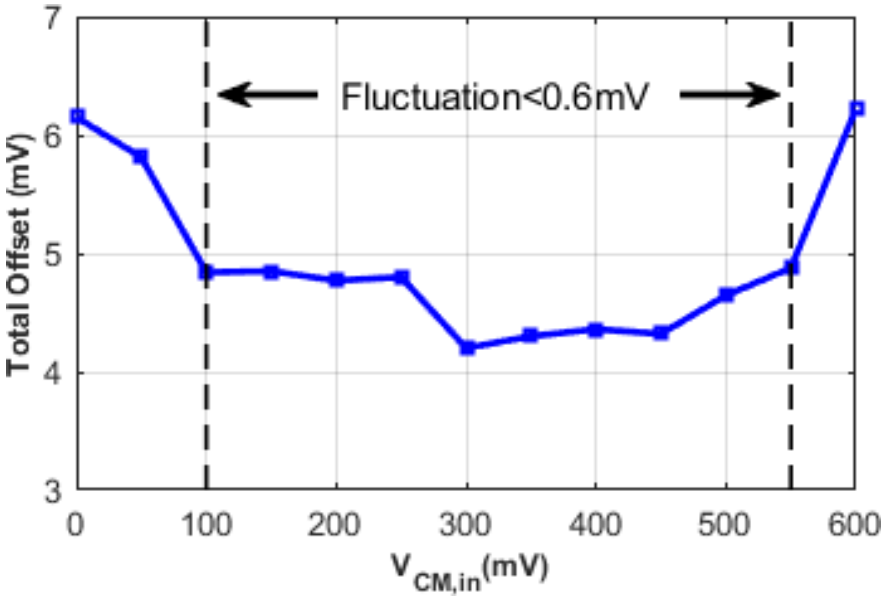
*Introduction:*For many energy-limited applications like energy harvesting systems, battery-operated systems, and implantable biomedical devices, operating in low-supply voltage is paramount. Comparators are the ubiquitous block of such applications mixed-signal circuit design [1, 2]. However, designing a high-performance comparator with low-supply voltage operation is very challenging. First, low supply voltage operation restricts comparator's common-mode input range, important for some ADCs like successive approximation register (SAR) and Flash ADC [3]. Next, once the supply voltage decreased, transistors operate mainly in the subthreshold region where transistors' threshold voltage offset contribution to total offset increases. Hence, a large transistor size is required, resulting in higher power and area consumption [4]. This is while the transistors' threshold voltage scaling could not succeed at the same rate of supply voltage in modern CMOS technologies, attaining a low comparison time is difficult[5].*Circuit Design:* Using bulk-driven transistor is the most popular technique when it comes to designing a low-supply voltage-operated comparator. A single-stage regenerative comparator is designed in [6] with this technique which has a limited input common-mode range. This limitation is resolved by the non-clocked bulk-driven comparator, implemented

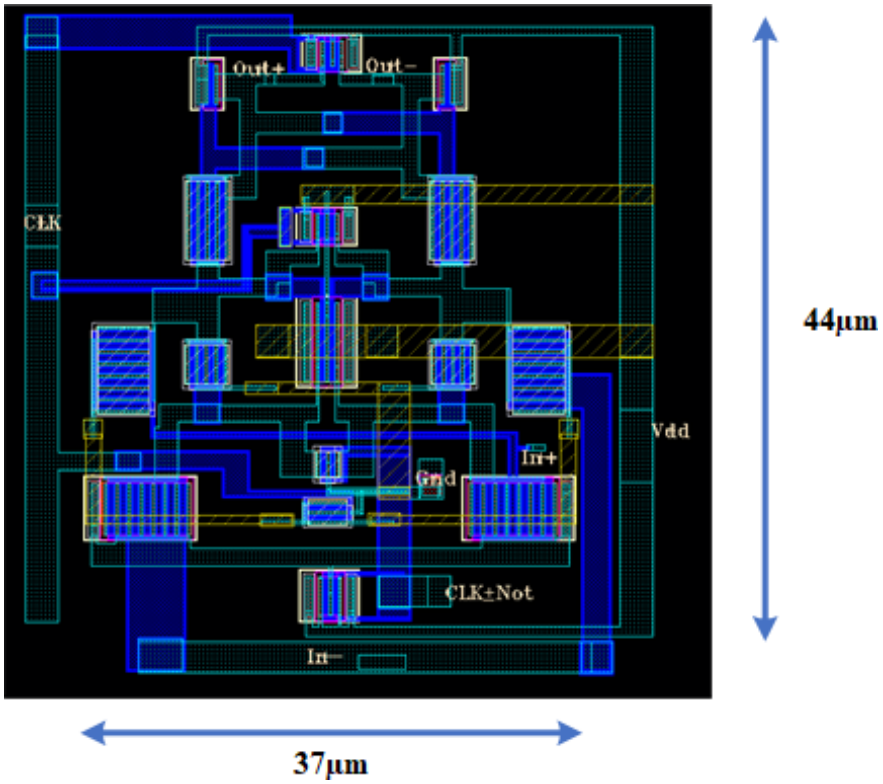
in [7]. Generally, this technique increases leakage currents and decreases the comparator's power efficiency. A rail-to-rail synthesizable comparator is pioneered in [8] which achieves low power consumption but a very long comparison time. In this work without complicating the design, a novel energy-efficient rail-to-rail two-stage high-speed and low offset regenerative comparator is presented.



The proposed comparator alongside main waveforms is illustrated in Figure 1. In the first stage, pre-amplifier, includes input transistorsM_{1-4}, and two tail transistors. The other transistors are included in the dynamic latch structure. M_{13} and M_{14} set up a positive feedback so-called "Thyristor" which has been used in some circuits [9]. As shown in Figure 1. b, during the reset phase, nodes O_{1+} and O_{1-} are discharged to the ground and nodes O_{2+} and O_{2-} are charged to Vdd by relative transistors. In other words, thyristors are off. Supposing $I_{n+} > I_{n-}$, as the evaluation phase starts node O_{1+} is charged much faster thanO_{1-} by input transistors M_{1-2}. Likewise, nodeO_{2+} is discharged faster than O_{2-} by input transistors M_{3-4}. It is only needed node O_{1+} is charged to v_{tn} or O_{2+} discharged to$Vdd - v_{\mathrm{tp}}$ where v_{tn} and $v_{\mathrm{tp}}$are the threshold voltages of PMOS and NMOS transistors. Then, in due time, the thyristor is activated and promptly flips its state. In this scenario, the left thyristor (M_{13} and M_{14}) of the comparator is activated sooner than the right one (M_{15} and M_{16}). So,M_9 is turning on sooner than M_{10} and dynamic latch provides the final outputs (Out+ and Out-). At low common-mode input voltages, PMOS input transistors (M_1, M_2) are accountable to activate thyristors and NMOS input transistors (M_3, M_4) are obligated to do the same task at the high common-mode input voltages.

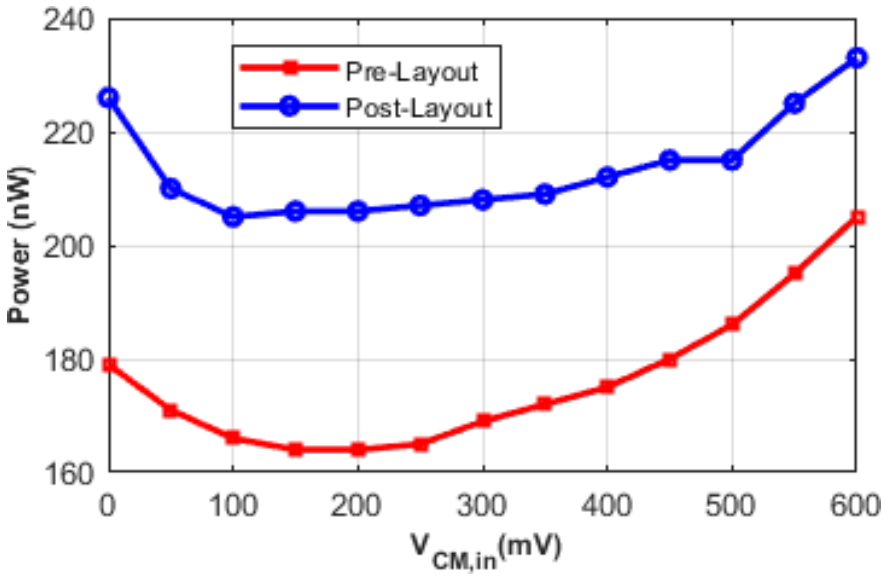
Results: The proposed comparator is designed in a standard 180nm CMOS technology with load capacitance of 2.5 fF implemented by MOM cap (which are not shown), with the operating frequency of $1MHz$ and $Vdd = 0.6V$. The layout of the circuit is shown in Figure 2. Transistors are designed with large sizes to attain low offset voltage which results in 37µm ×44 µm area occupation.





The total input-referred offset (3std+mean) of the comparator which is performed by 1000 runs of Monte Carlo simulation, is shown in Figure 3. The total offset voltage is less than 6.2mV within entire common-mode rang. The offset fluctuation within common-mode range is about 2mV. However, for limited range offset fluctuation is decreased. For instance, for $V_{CM,in} = (100 - 550)\,\mathrm{mV}$ offset fluctuation is less than 0.6mV.

The delay of the comparator which calculated at$|\text{Out}_+ - \text{Out}_-| = 0.5$ Vdd is shown in Figure 4 for different input common mode voltages and ΔVin=10mV. The results corroborate that maximum delay occurs at$V_{CM,in} = 0.5Vdd$ where input transistors (M_{1-4}) are partially turned on.



The power consumption of the comparator is also shown in Figure 5. The proposed circuit consumes less than 230nW of power within entire common-mode range.

To evaluate the performance of the comparator over PVT variations, simulation results are shown in Table 1. From the table for worst-case scenario (Vcm=300mV), the maximum delay is observed at SS corner.

Process	TT	FF	SS	FS	SF
Temperature ()	27	-20	85	27	27
Delay(ns)	28	10	69	19	31
Power (nW)	208	246	215	207	275
Offset(mV)	4.2	3.8	4.87	3.9	5.17

Table 1: PVT simulation results, Vcm=300mV.

The performance results of the proposed comparator alongside other works are summarized in Table 2. Since achieving low offset voltage is very power hungry in

Comparator	[6][a]	[7][b]	[8][b]	This work[a]
Tech (nm)	180	130	180	180
Supply(V)	0.6	0.6	0.6	0.6
$\mathbf{f_{op}}$**(KHz)**	200	1000	10	1000
Power(nW)	144	1300	1.95	230
Delay(ns)	118.2	-	740	28
Total Offset(mV)	14.6	6.02	23	6.2
Common-mode range	(0.3-0.6)	(0-0.6)	(0-0.6)	(0-0.6)
Area($\mu\mathbf{m^2}$)	-	410	900	1628
FOM (fJ.V)	10.5	7.8	4.48	1.42

Table 2: Comparison table.

a: simulation b: measurement FOM= (power × offset)/fop

comparator design, in order to genuinely compare the performance of the comparators, the FOM introduced in [5] is utilized which the energy of comparison multiplied by offset voltage. As can be seen, the proposed comparator achieves the best FOM in comparison with similar works.

Conclusion: An energy efficient two-stage regenerative comparator is presented. The second stage utilizes thyristor-based dynamic latch with enable rail-to-rail operation of the comparator. The presented comparator is realized in circuit level using a 180nm standard CMOS technology. The post-layout simulation results corroborate that power and delay of the comparator is no more than 230nW and 28nW with 0.6V supply voltage and 1MHz clock frequency. The total offset of the comparator within rail-to-rail common-mode range, is less than 6.2mV. Considering the overall performance, the proposed comparator attained the best FOM in comparison with other state-of-the-art works. The proposed comparator is well suited to be utilized in energy harvesting systems and low voltage ADCs.

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