Design of capacitor-less LDO regulator with NLRSCR based high robustness ESD protection circuit using dynamic feedback loop for low-voltage applications

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Abstract

The capacitor-less low dropout voltage regulator applied to mobile devices increases the power consumption due to the continuously exposed peak voltage. The dynamic feedback loop for the LDO regulator proposed in this study can provide a function to stably control the peak voltage regardless of the change in the load current. The performance of chip layout maintains an output voltage of 3V with a battery input voltage of 3.3-4.5V and a load current of 350mA. The peak voltage was maintained the undershoot voltage of 30mV and the overshoot of 33mV regardless of the change in the load current. In addition, circuit damage due to ESD (Electro Static Discharge) may occur frequently due to the increase of applications using low voltage along with miniaturization and integration of IC. This is an important factor affecting the overall reliability related to the productivity and stability. As a result, it was confirmed that the proposed LDO regulator secures high reliability at low voltage by applying the ESD protection circuit of the NLRSCR structure.

Design of capacitor-less LDO regulator with NLRSCR based high robustness ESD protection circuit using dynamic feedback loop for low-voltage applications

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Proposed LDO regulator with dynamic feedback loop: Mobile and wearable devices require dozens of LDO regulators to handle the various voltages and load currents. The LDO regulator proposed in this letter is designed to maintain a stable voltage by applying an additional dynamic feedback loop to respond sensitively to changes in load-based output voltage [1, 2]. Figure 1 shows a block diagram of a proposed LDO regulator

with ESD protection circuit. Therefore, the proposed LDO regulator has effectively improved the reliability and transient response characteristics with a dynamic feedback structure and an NLRSCR ESD protection circuit structure. Figure 2 shows the behavior and current path of the dynamic feedback structure in the undershoot condition. The proposed LDO regulator with the dynamic feedback structure priorly changes the feedback voltage by the instantaneous change of load current.

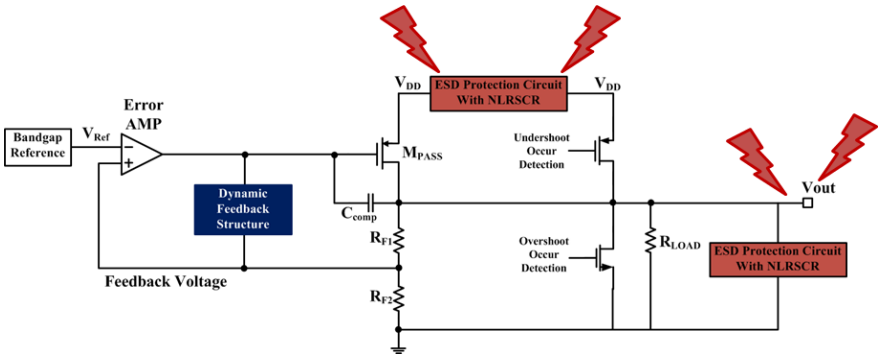

Fig 1 *Capacitor-less proposed LDO regulator with ESD protection circuit based on NLRSCR*

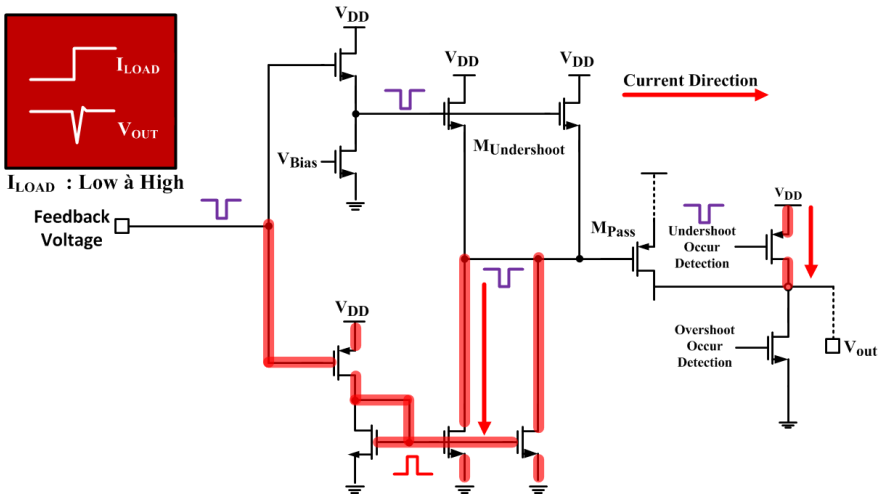

Fig 2 *Dynamic feedback loop according to undershoot situation*

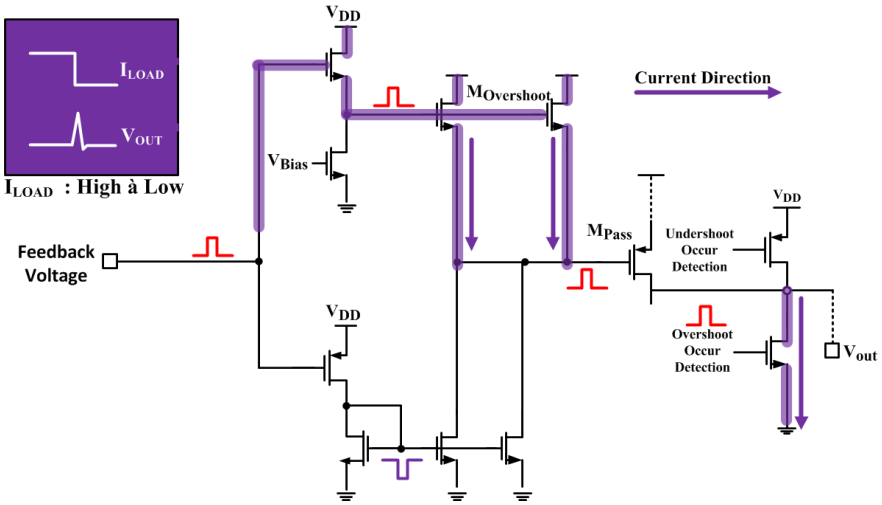

Fig 3 *Dynamic feedback loop according to overshoot situation*

The changed feedback voltage acts in the current discharge path to effectively reduce the gate terminal voltage of the pass transistor while the output stage supplies the additional current. Figure 3 also shows the behavior and current path of the dynamic feedback structure in the overshoot condition. The proposed LDO regulator with a dynamic feedback structure forms the current discharge path so that the changed feedback voltage due to the instantaneous dissipated load current effectively increases the gate terminal voltage of the pass transistor while the output stage discharges an additional current. The conventional LDO regulators with the single feedback generate sensitive to load current the output voltages. However, it can be predicted that the proposed LDO regulator with dynamic feedback function by forming three feedback loops effectively controls the output voltage more [3, 4, 5].

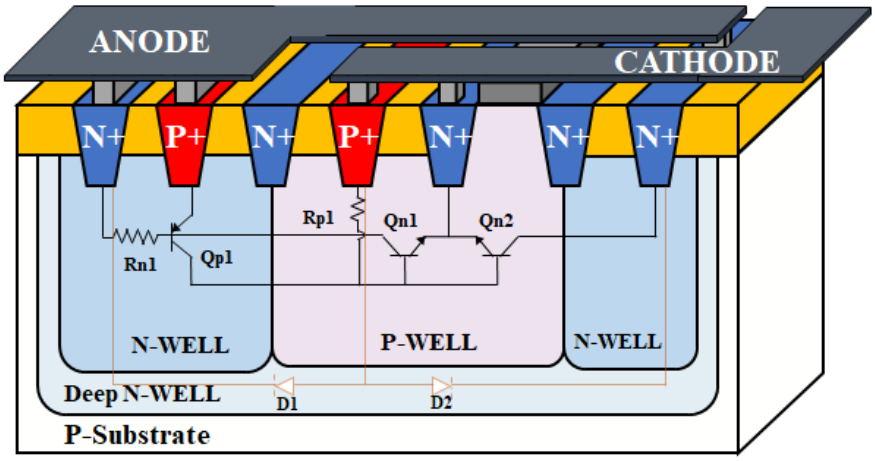

Fig 4 *NLRSCR (N-type Low Ron Silicon Control Rectifier)*

NLRSCR structure ESD protection circuit: Figure 4 shows the structure with the equivalent schematic of the proposed NLRSCR ESD protection circuit. The proposed NLRSCR ESD protection circuit has an additional NPN parasitic bipolar transistor Qn1 with a shorter discharge path and larger current gain than the NPN parasitic bipolar transistor for structural design. The base region of the NPN parasitic bipolar transistor Qn2 is minimized to the gate region as compared to the conventional SCR LRSCR PNP parasitic

bipolar transistor. The result is a lower trigger voltage, better margin of error, and lower on-resistance. The operating principle of the proposed ESD protection circuit is as follows. Under normal operating conditions, the junction between the N + bridge region and the P well region is reverse biased and ESD protection does not work. When an ESD surge is applied to the anode region, the potential in both N-well regions increases, and when the potential reaches the threshold, avalanche breakdown occurs in both the N + bridge region and the P-well region, resulting in positive electron. Therefore, a pair of holes is generated. The generated hole current flows into the P + cathode region, which increases the potential in the P well region. When a forward junction is formed between the P-well region and the N + cathode region, two NPN parasitic bipolar transistors Qn1 and Qn2 connected in parallel are turned on, and the current flowing through the NPN parasitic bipolar transistor turns on the PNP parasitic bipolar transistor. Due to this, transistor Qp1 is turned on. Therefore, the three BJTs Qn1, Qn2, and Qp1 form an SCR loop and discharge the ESD surge [6, 7, 8].

Measurement result: The proposed LDO regulator was built using 0.18-μm BCD process as shown in Figure 5. The proposed LDO regulator configured as shown in Figure 5 was manufactured to verify the improvement of the peak voltage regardless of the load current by using a dynamic feedback loop, and of the electrical characteristics and the current driving capability of the NLRSCR protection circuit. Figures 6 and 7 show the measurement results of the transient response characteristics of the proposed LDO regulator. The proposed LDO regulator verified that the peak voltage value due to the load current was improved due to the influence of the dynamic feedback loop. An undershoot voltage of 30 mV and an overshoot voltage of 33 mV were secured when a load current of 350 mA was generated. As a result, we have verified that the proposed dynamic feedback loop of the LDO regulator effectively

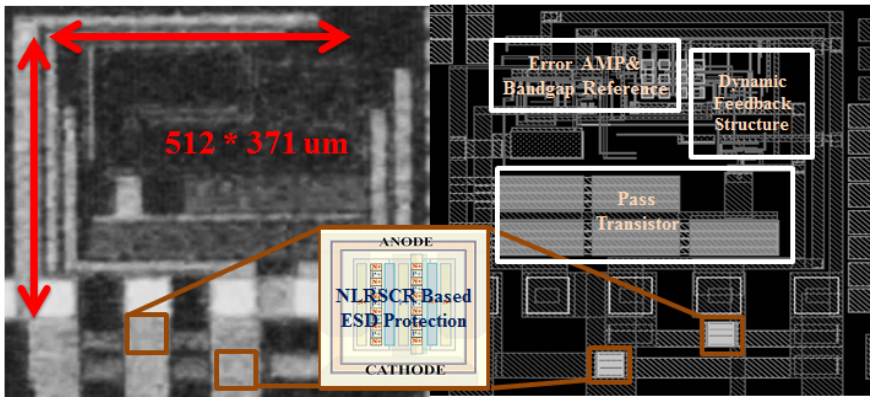

Fig 5 Chip layout of dynamic feedback loop LDO regulator including NLRSCR ESD protection circuit

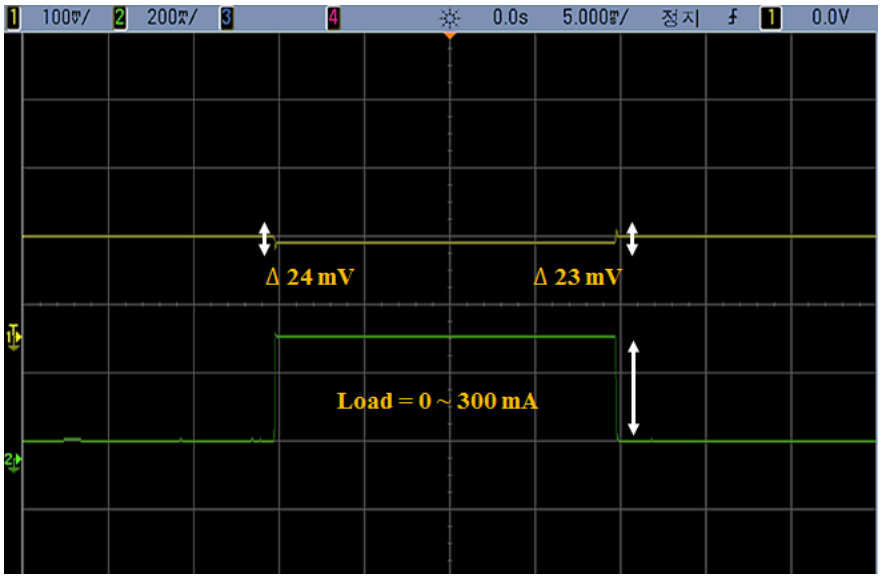

Fig 6 Transient response measurement result of dynamic feedback loop LDO regulator

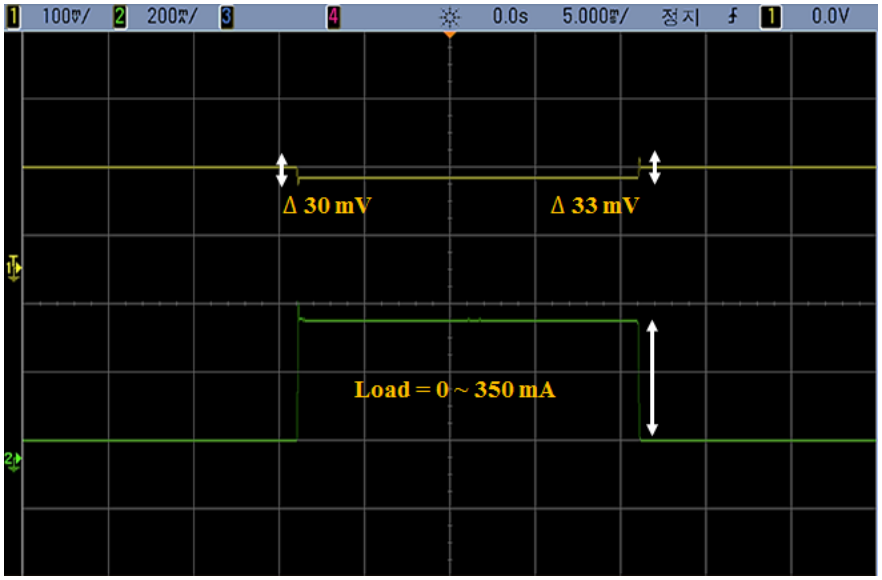

Fig 7 Transient response measurement result of dynamic feedback loop LDO regulator

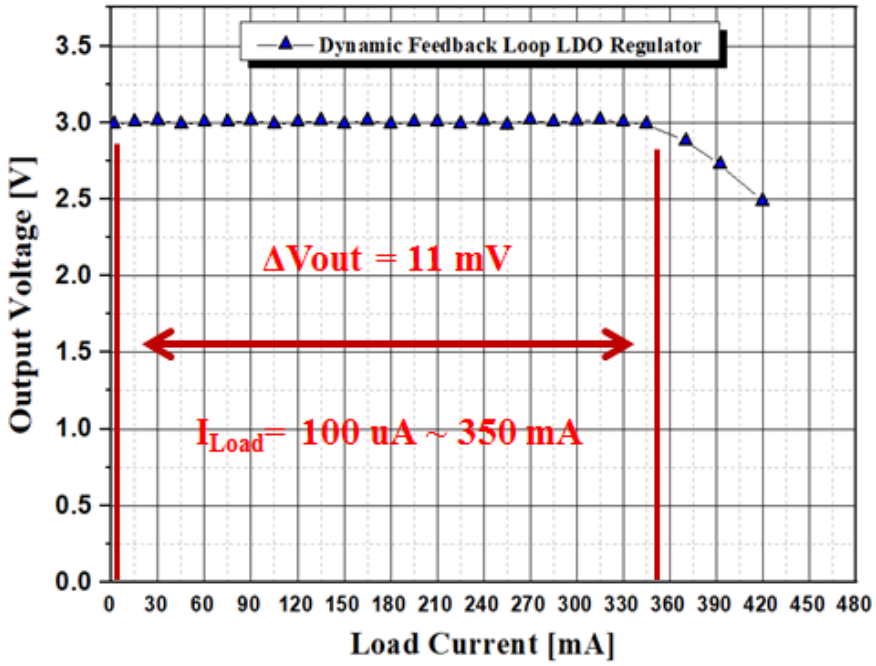

Fig 8 Load regulation measurement result of dynamic feedback loop LDO regulator

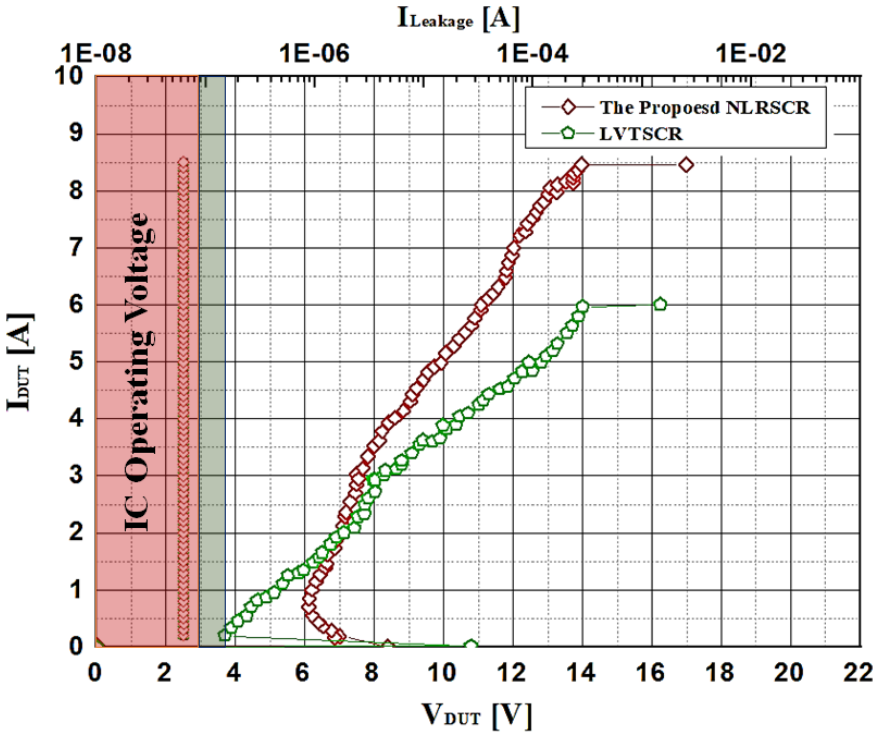

Fig 9 TLP I–V characteristic curves of conventional LVTSCR and the proposed NLRSCR ESD protection circuit

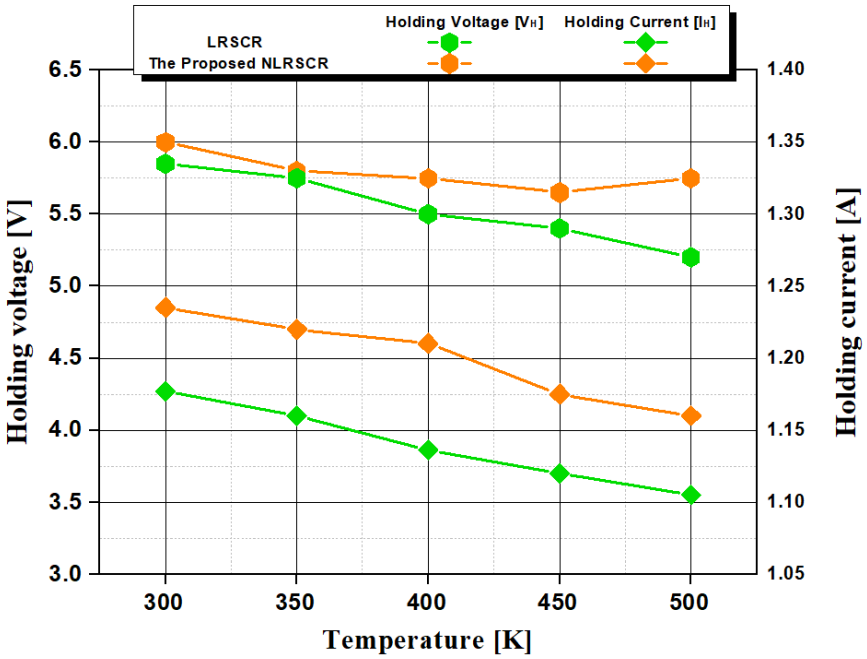

Fig 10 Electrical characteristic of proposed NLRSCR ESD protection circuit at high temperature (300–500 K)

controls the output voltage by forming an additional feedback loop. Figure 8 shows the output voltage along load current applied to the proposed LDO regulator. The LDO regulator must always have the function to maintain a stable voltage regardless of the rate of change of the load current. Figure 8 shows that the proposed LDO regulator maintains an output voltage difference of 11mV while the load current is changed up to 350mA. According to Figure 9, the IV characteristics were measured using TLP. The hold voltage of LVTSCR is 3.68V, which invades the operating area of the internal IC and may cause problems such as latch-up. The proposed NLRSCR ESD protection circuit has a trigger voltage of 8.4V and a holding voltage of 6V, so this trigger voltage value is lower than 10.8V for LVTSCR and is suitable for the 5V ESD design window. And also, according to the measurement result at a high temperature of 500K shows that the conventional LRSCR has a maintenance voltage of 5.2V and a secondary trigger current of 5.02A as shown in Figure 10. On the other hand, the holding voltage of the proposed NLRSCR ESD protection circuit is 5.5V. The secondary trigger current is still as high as 7.04 A, which is the proposed NLRSCR ESD protection circuit with superior thermal reliability and high temperature characteristics compared to conventional LRSCR.

Conclusion: The voltage and current required by various systems must be provided in a stable manner regardless of external factors. The LDO regulator with the dynamic feedback loop proposed in this study is designed to supply additional current or form a discharge path according to the load current. As a result, it was confirmed that the proposed LDO regulator can effectively controls the output voltage regardless of the change rate of the load current. Also, the proposed NLRSCR ESD protection circuit has verified superior thermal reliability and high temperature characteristics compared to conventional LRSCR. The proposed LDO regulator has been verified to optimize the power consumption for low voltage applications and to ensure ESD immunity and reliability.

Acknowledgments:

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